2019 IWLPC Program

Tuesday, October 22

7:30 AM	**REGISTRATION OPENS**		
8:45 AM	**OPENING COMMENTS/AWARDS** Chris Scanlan JCET		
9:00 AM	**KEYNOTE: The OSAT's Dilemma and the Future** Presenter: Choon Heung Lee, Ph.D., CTO, JCET		
10:00 AM	**BREAK IN THE EXHIBIT HALL**		
	WLP Track (Room: Oak)	3D Track (Room: Pine)	Advanced Manufacturing Track (Room: Cedar)
	Session 1: Advanced Wafer-Level Packaging Technology	Session 2: Design	Session 3: Process Materials
10:30 AM	**Highly Integrated SiP for Mobile Devices** JungHwa Kim, P.Eng., Samsung Electronics	**System Co-Design Inclusive of Connectivity for 3DIC and Wafer-Level Packaging** Narayanan TV, Ph.D, Cadence Design Systems	**The Growing Application Field of Laser Debonding: From Advanced Packaging to Future Nanoelectronics** Alain Phommahaxay, Ph.D., imec
11:00 AM	**Semiconductor-on-Polymer, the Evolution of Thin IC Packaging** Douglas Hackler, American Semiconductor	**Shift-Left Verification in HDAP Design** Christopher Cone, Mentor, A Siemens Business	**Advanced Low-Loss and High-Density Photosensitive Dielectric Material for RF/Millimeter-Wave Applications** Hirokazu Ito, JSR Corporation
11:30 AM	**Process Development for Flip-Chip Bonding with Different Bump Compositions** Samuel Massa, MS, Northrop Grumman	**Leveraging the Best of Package and IC Design for System Enablement** Bill Acito, Cadence Design Systems	**Glass Solutions for Wafer-Level Packaging** Aric Shorey, Mosaic Microsystems
12:00 PM	**High Density Flex and Thin Chip Embedding Technology for Polymeric Interposer and Sensor Packaging Applications** Kai Zoschke, Fraunhofer IZM	**Advanced RF Packaging Technology Trends, from WLP and 3D Integration to 5G and mmWave Applications** Stéphane Elisabeth, Ph.D., System Plus Consulting	**Advanced Black Resist Processing and Optimized Lithographic Patterning for Novel Photonic Devices** Bozena Matuskova, M.Eng., EV Group
12:30 PM	**LUNCH**		
	WLP Track	3D Track	Advanced Manufacturing Track
	Session 4: Reliability and Metrology	Session 5: Characterization and Test	Session 6: Process Equipment
2:00 PM	**Reliability and Performance of Wafer Level Fan Out Package for Automotive Radar** Walter Hartner, Ph.D., Infineon Technologies	**Thermomechanical Characterization of Polymer Thin Films. Application for the Conception and the Manufacturing of a 3D Interposer** Lionel Vignoud, Ph.D., Université Grenoble Alpes, CEA-Leti	**FOPLP Lithography Solutions to Overcome Die Placement Error, Predict Yield, Increase Throughput and Reduce Cost** Keith Best, Rudolph Technologies
2:30 PM	**System for Measuring Three-Dimensional Micro-Structure Based on Phase Shifting Fringe Projection** Chia-Hung Cho, P.Eng., Industrial Technology Research Institute	**Non-Destructive 3D X-Ray Characterization of Application Processor Panel Level Pacakage Used in Galaxy Smartwatch** Thomas Gregorich, ZEISS PCS	**An Overview About the Excimer Laser Ablation of Different Polymers and Their Application for Wafer and Panel Level Packaging** Robert Gernhardt, Fraunhofer IZM
3:00 PM	**Ultra-Low Warpage and Excellent Filling Ability Liquid MUF for Advanced Fan-Out Wafer Level Package** Yohei Nishimura, Panasonic Corporation	**Application of Acoustic Metrology for In-line Microbump Process Monitoring in Advanced Packaging** Robin Mair, Rudolph Technologies	**Functional Inkjet Printing Equipment: A Set of Features Leading to Productive Results** Luca Gautero, Ph.D., Meyer Burger (Netherlands) BV
3:30 PM	**BREAK IN THE EXHIBIT HALL**		
4:00 PM	**PANEL DISCUSSION: Large Organic Panels: How Can We Achieve 2µm L/S?** Moderators: Jan Vardaman, President & Founder, TechSearch International, Inc.; Tanja Braun, Ph.D., Fraunhofer IZM Panelists: John Hunt, ASE; Joseph Dang, AT&S; Keith Best, Rudolph Technologies; Tim Olson, Deca Technologies		
5:00 PM-6:00 PM	**NETWORKING RECEPTION**		

Wednesday, October 23

7:00 AM	**REGISTRATION OPENS**		
8:00 AM	**OPENING COMMENTS** Chris Scanlan JCET Group		
8:15 AM	**BREAKFAST KEYNOTE: Slowdown: When Did it Start … What Drove it … When Will the Recovery Come** Presenter: G. Dan Hutcheson, CEO, VLSIresearch		
9:15 AM	**BREAK**		
	WLP Track (Room: Oak)	3D Track (Room: Pine)	Advanced Manufacturing Track (Room: Cedar)
	Session 7: Fan Out Wafer-Level Packaging (FO-WLP)	Session 8: Wafer Bonding	Session 9: Wafer & Panel Test/Metrology 1
9:30 AM	**Panel Level Packaging for Component Integration of an Energy Harvesting System** Tanja Braun, Ph.D., Fraunhofer IZM	**Novel Temporary Bonding and Debonding Solutions Enabling an Ultrahigh Interconnect Density FO-WLP Structure Assembly with Quasi-Zero Die Shift** Dimitrios Velenis, Ph.D., imec	**Evaluation of a Spring Probe Card Solution for 5G WLCSP Applications** Krzysztof Dabrowiecki, MSc, Feinmetall GmbH
10:00 AM	**Advanced Fan Out Wafer-Level Package Development for Small Form Factor and High-Performance Microcontroller Applications** Gaurav Sharma, Ph.D., NXP Semiconductor	**Chip to Wafer Hybrid Bonding with Cu Interconnect: High Volume Manufacturing Process Compatibility Study** Guilian Gao, Ph.D., Xperi	**Wave Front Phase Imaging of Wafer Geometry Using High Pass Filtering for Improved Resolution** Jan Gaudestad, Wooptix
10:30 AM	**Latest Technology of Epoxy Molding Compound (EMC) for FO-WLP** Tatsuya Kazama, Sumitomo Bakelite Co., Ltd.	**Recent Developments in Fine-Pitch Wafer-to-Wafer Hybrid Bonding with Copper Interconnect** Jeremy Theil, Ph.D., MS, Xperi	**Recent Breakthroughs in Tight Pitch Laser Microdrilling for MEMS Guide Plates** Alan Ferguson, Ph.D., Oxford Lasers, Ltd.
11:00 AM	**BREAK IN EXHIBIT HALL**		
	WLP Track	3D Track	Advanced Manufacturing Track
	Session 10: Advanced Package Processing	Session 11: Processing for Fan-Out	Session 12: Wafer & Panel Test/Metrology 2
11:30 AM	**Report on an Integrated Technique for Solder Ball Reflow and Flux Clean** Gary Hillman, S-Cubed	**Processing and Memory Partitioning Enabled by Low Cost Flip-Chip Stacking** Fabian Hopsch, Fraunhofer EAS	**The Latest in XRF Coatings Analysis Equipment for Micro-Scale Semiconductor Packaging** Matt Kreiner, Hitachi High-Tech
12:00 PM	**Defect-Free Electroplating of High Aspect Ratio Through Silicon Vias: Role of Size and Aspect Ratio** Sridhar Narayanaswamy, Ph.D., Institute of High Performance Computing	**The Effect of Cu Target Pad Roughness on the Growth Mode and Void Formation in Electroless Cu Films** Sebastian Zarwell, Ph.D., Atotech Deutschland GmbH	**Validating Die Crack Inspection with Topography Based Image Sensor** Woo Young Han, Rudolph Technologies
12:30 PM	**Heterogeneous Integration Solutions for HPC Application by Using FO-MCM Chip Last Platform** Pin-Jing Su, P.Eng., SPIL	**Innovative Plating for Heterogeneous Integration** Richard Hollman, ASM NEXX	**High Resolution Automatic X-Ray Inspection for Continuous Monitoring of Advanced Package Assembly** Scott Jewler, SVXR, Inc.
1:00 PM	**LUNCH**		
	WLP Track	3D Track	
	Session 13: Advanced BE Wafer Process	Session 14: Processes for FOWLP	
2:00 PM	**Improved Semiconductor Device Reliability from Plasma Dicing** Richard Barnett, SPTS Technologies Ltd	**Solutions for Advanced Heterogeneous Integration and Fan-Out Processes** Doug Shelton, Canon USA	
2:30 PM	**A Unique and Robust Technique to Eliminate Warpage for FOWLP and FOPLP During the Thermal Debonding Process** Debbie Claire Sanchez, P.Eng., ERS electronic GmbH	**Enabling Heterogeneous Integration for Next Generation Fan-Out Applications Using Full-Field Projection Scanning** Fabian Benthaus, SÜSS MicroTec	
3:00 PM	**Thermal Laser Separation (TLS) with Deep Scribe for Silicon Wafer Dicing** Christian Belgardt, 3D-Micromac AG	**Producing Vias in Photosensitive Polyimide Passivation Layers for Fan Out PLP Through the Integration of an Advanced Lithography System with a Novel Nozzle-Less Spray Coating Technology** Stuart Erickson, Ultrasonic Systems, Inc	
3:30 PM	**BREAK IN EXHIBIT HALL**		
4:00 PM	**KEYNOTE: A Borderless Future for Electronic Interconnect** Presenter: Tim Olson, Founder & CTO, Deca Technologies		
5:00 PM	**Closing Comments**		

Thursday, October 24

	Professional Development Courses	
	Donner Pass Ballroom	Siskiyou Ballroom
8:30 AM	PDC1: Evolution from Basic to Advanced Fan Out John Hunt, ASE	PDC2: Polymers in Wafer Level Packaging Jeff Gotro, Ph.D., InnoCentrix, LLC
1:30 PM	PDC3: Modeling Failure Modes for Chip Package Interactions and Package Level Reliability Gilad Sharon, Ph.D., ANSYS	PDC4: Fan-Out Wafer/Panel-Level Packaging and Heterogeneous Integrations John Lau, Ph.D., Unimicron Technology Corporation