Session at a Glance

7:00am	**Registration Opens**		
	Tuesday, October 18, 2016		
	Session 1 **WLP - 8:00am-10:00am (Oak)**	**Session 2** **3D - 8:00am-10:00am (Pine)**	**Session 3** **Manufacturing - 8:00am-10:00am (Cedar)**
	Fan Out WLP Applications Chair: Rey Alvarado, Qualcomm Technologies, Inc. Co-Chair: Vivek Dutta, Ormet Circuits	**Advanced Packaging Schemes** Chair: Herb Reiter, eda 2 asic Consulting, Inc. Co-Chair: Amandine Pizzagalli, Yole Développement	**Productivity Solutions I** Chair: Steffen Kröhnert, NANIUM S.A. Co-Chair: Bernard Adams, STATS ChipPAC
8:00am	Fabrication and Reliability of a Thermally Enhanced WLFO Demonstrator *Eoin O'Toole, NANIUM S.A.*	BVA Enabled Low-Profile, High Density Fan-Out Wafer-Level PoP *Min Tao, Ph.D., Invensas*	Wafer Level Process Formation of a Polymer Isolated Chip Scale Package *Harry Gee, ON Semiconductor*
8:30am	Wafer-Level System in Packaging (SiP) Technologies as 2D, 3D Module/System Integration Solution Jay Kim, *nepes Corporation*	Performance limits of stacked FO WLPs and their Mitigation *Dev Gupta, Ph.D., APSTL*	Quality Pressures in Advanced Packaging *Selim Nahas, Applied Materials; Yao Hong Tan, GLOBALFOUNDRIES; Manan Dedhia, Analog Devices*
9:00am	FOWLP: Comparison & Highlight on the Latest Technologies Trends *Romain Fraux, Systems Plus Consulting*	System-in-Package (SiP) Assembly vs. Solder Paste Attributes *Sze Pei Lim, Indium Corporation*	A Practical Approach to Test Through Silicon Vias (TSV) *Gerard John, Amkor Technology*
9:30am	Silicon Wafer Integrated Fan-Out Technology (SWIFT) *Bora Baloglu, Ph.D., Amkor Technology*	Process Controls for Advanced Thermocompression Bonding *Tom Strothmann, Kulicke & Soffa*	Direct Bond Interconnect (DBI®) Technology as an Alternative to Thermal Compression Bonding *Guilian Gao, Ph.D., Invensas Corporation*
10:00am	**Refreshment Break & Interactive Presentations (10:00am-1:30pm)** **Exhibit Hall** Interactive Presentation Chair: Dale Gee		
10:45am	**Welcome Comments** Oak Ballroom (2nd Floor) Curtis Zwenger, Amkor Technology IWLPC General Chair		
11:00am	**KEYNOTE ADDRESS:** Klaus-Dieter Lang, Ph.D., Fraunhofer IZM Advanced Technology Platforms for Next Generation of Smart Systems Chair: Curtis Zwenger, Amkor Technology		
12:00pm	**Lunch Break**		
	Session 4 **WLP - 1:30pm-3:30pm (Oak)**	**Session 5** **3D - 1:30pm-3:30pm (Pine)**	**Session 6** **Manufacturing - 1:30pm-3:30pm (Cedar)**
	WLP Process Developments Chair: Vivek Dutta, Ormet Circuits Co-Chair: Rey Alvarado, Qualcomm Technologies, Inc.	**3D Enablers and Considerations** Chair: Laurette Nacamulli, Dow Chemical Co Co-Chair: Arun Aiyer, Ph.D., Anjay Technology	**Productivity Solutions II** Chair: Suresh Jayaraman, Amkor Technology Co-Chair: Selim Nahas, Applied Materials
1:30pm	The Novel Liquid Molding Compound for Fan-Out Wafer-Level Package *Katsushi Kan, Nagase ChemteX Corporation*	High Speed Interfaces between Chips Mounted with Different Integration Technologies on an Interposer *Andy Heinig, Fraunhofer IIS/EAS*	New Laser Multi Beam Full Cut Dicing of Wafer-Level Chip-Scale Packages (Fan In) *Richard Boulanger , ASMPT ALSI*
2:00pm	Development of Bump Support Film (BSF) for Improving Package Reliability of WLCSP *Masanori Yamagishi, Lintec Corporation*	Miniaturizing RF Module Using Glass Interposer Technology *Ganesh Bhatt, TE Connectivity*	Rapid Polymer Curing for Improved Manufacturing Metrics *Jackie Lyn Yusi, Deca Technologies*
2:30pm	Electroplated Nano Twinned Copper for Wafer-Level Package *Stream Chung, Ph.D., Chemleader*	3D-TSV Assembly: Package Architectures and Trade-offs *Paul Silvestri, Amkor Technology*	Key Criteria for Successful Integration of Laser Debonding *Elizabeth Brandl, EV Group*
3:00pm	Full-field Projection Scanner Patterning Resolution and Overlay Performance *Habib Hichri, Ph.D., SUSS MicroTec Photonic Systems Inc.*	Cost Analysis of Die Assembly for 2.5D and 3D Packaging *Chet Palesko, SavanSys Solutions LLC*	Wafer-Level Encapsulation-An Alternative Format for Discrete Packaging: Its Challenges and Solutions *Eric Kuah, DBA, SM Technology Singapore Pte Ltd*
3:30pm	**Refreshment Break** Exhibit Hall		
4:15pm	**Panel Discussion-The Role for Large-Area Panel Processing in the Quest for Low-Cost FOWLP** Oak Ballroom (2nd Floor) Moderator: Jan Vardaman, TechSearch International, Inc. Chair: John Lannon, Ph.D., Micross Advanced Interconnect Technology, LLC **Panelists:** Bernard Adams, STATS ChipPAC Inc. David Butler, SPTS Technologies Choon Lee, Lam Research Urmi Ray, Qualcomm Technologies, Inc. Chris Scalan, Deca Technologies		
5:30pm-7:00pm	**Reception**		

NEW! Interactive Presentations

Tuesday, October 18, 2016

10:00am - 1:30pm

Study on a Formulated Flux for Ultra-Fine Flip Chip Interconnect
Roderick Chen, SHENMAO America, Inc.

Bridging the Gap: A Cohesive Design to Sign-off Platform for Wafer-Level Packaging
John Ferguson, Mentor Graphics

High-Performance, Low-Cost Photoresist Strip for Advanced Packaging Applications
George Chiaverini ,Veeco Precision Surface Processing; Amy Lujan, SavanSys Solutions LLC

Laminatable Positive-Tone Photosensitive Polyimide
Masao Tomikawa, Ph.D., Toray Industries, Inc.

Board Level Reliability of Automotive eWLB (Embedded Wafer-Level BGA)
Bernard Adams, STATS ChipPAC Inc.

7:00am	**Registration Opens**		
	Wednesday, October 19, 2016		
8:30am	**KEYNOTE ADDRESS: Rao R. Tummala, Ph.D., Georgia Institute of Technology** Promise and Future of Embedding and Fan-Out Technologies Chair: Chris Scanlan, Deca Technologies		
9:30am	**Refreshment Break** Exhibit Hall		
	Session 7	**Session 8**	**Session 9**
	WLP - 10:00am-12:00pm (Oak)	**3D - 10:00am-12:00pm (Pine)**	**MEMS - 10:00am-12:00pm (Cedar)**
	Fan in & Fan Out Modeling and Simulations Chair: Jie Gong, Ph.D., KLA-Tencor Co-Chair: Luu Nguyen, Texas Instruments	**Metrology and Process Control** Chair: Arun Aiyer, Ph.D., Anjay Technology Co-Chair: Tom Strothmann, Kulicke & Soffa	**MEMS Bonding Landscape** Chair: Garrett Oakes, EV Group Co-Chair: John Lannon, Ph.D., Micross Advanced Interconnect Technology, LLC
10:00am	Chip/Package Co-Analysis for Thermal-Induced Stress of Fan-Out Wafer Level Packaging *Stephen Pan, Ph.D., ANSYS, Inc.*	Application of 3D X-Ray Microscopy for 3D IC Process Development *Stephen Kelly, Zeiss*	AuSn Eutectic Bonding for Wafer- Level Hermetic Packaging Using a Novel AuSn Patterning Process *Hiroyuki Ishida, SUSS MicroTec KK*
10:30am	SIP Assembly with Sintering Paste in FO-WLP *Catherine Shearer, Ormet Circuits, Inc.*	Sub-μM 3D Metrology for RDL Structures in FO-WLP and Advanced Packaging Using Multi-Sensor Interferometry *Moritz Jurgschat, Sentronics Metrology*	3D Wafer- Level Packaging for MEMS by using a Via Middle Approach based on Copper Through Silicon Vias Together with Copper Thermo-Compression Bonding *Lutz Hofmann, Fraunhofer ENAS*
11:00am	Understanding and Solving the Challenges of Chip to Package Co-Design for FOWLP *William Acito, Cadence Design Systems*	Advanced Detection and Removal Method of Polymer Residues on Semiconductor Substrates *Helene Richter, Ph.D., FhG IISB Erlangen*	Advances and Applications of Gold Electroplating to Semiconductor Devices *Lynne Michaelson, Ph.D., Technic Inc.*
11:30am	Ultrathin WLFO *Eoin O'Toole, NANIUM S.A.*	Ultra Thin Substrate Assembly Challenges for Advanced Flip Chip Package *Nokibul Islam, STATS ChipPAC Inc.*	Novel WLCSP Technology Solution for Fusion Device of CMOS Integrated Circuit with MEMS *Takahide Murayama, ULVAC, Inc.*
12:00pm	**Lunch Break**		
1:30pm	**Panel Discussion - Chip-Package Interaction (CPI) Challenges and Solutions for WLP and FOWLP** Oak Ballroom (2nd Floor) Moderator: Urmi Ray, Qualcomm Technologies, Inc. Chair: Curtis Zwenger, Amkor Technology **Panelists:** Paul Silvestri, Amkor Technology Mark Gerber, ASE Paul Mescher, Microsoft Jan Vardaman, TechSearch International, Inc. Luu Nguyen, Texas Instruments		
2:30pm	**Refreshment Break** Exhibit Hall		
	Session 10	**Session 11**	**Session 12**
	WLP - 3:15pm-5:15pm (Oak)	**3D - 3:15pm-5:15pm (Pine)**	**MEMS - 3:15pm-5:15pm (Cedar)**
	Fan-Out WLP Advances Chair: Kevin Demartini, HD Microsystems Co-Chair: Jie Gong, KLA-Tencor	**Processing: Handling, Stacking and Bonding** Chair: Peter Ramm, Ph.D., Fraunhofer EMFT Co-Chair: Kathy Cook, Tessera	**MEMS and Sensor Packaging Solutions** Chair: John Lannon, Ph.D., Micross Advanced Interconnect Technology, LLC Co-Chair: Garrett Oakes, EV Group
3:15pm	Development of High Density Fan-Out Package Platform for High Performance and RF Applications *Gaurav Sharma, Ph.D., GLOBALFOUNDRIES*	Low Cost Electrical Interconnect for 3D Fan-Out Wafer- Level Packaging *Ivy Qin, Ph.D., Kulicke & Soffa*	Patterned Adhesive Transfer for Wafer-Level Packaging Applications *Elizabeth Brandl, EV Group*
3:45pm	Advanced Packaging Lithography and Inspection Solutions for Next Generation FOWLP/FOPLP Processing *Keith Best, Rudolph Technologies*	Thin Wafer HandlingTechnologies for TSV Packaging *Amandine Pizzagalli, Yole Développement*	Wafer-Level Vacuum Packaging of Microbolometer-based Infared Imagers *Allan Hilton, RTI International*
4:15pm	High Productivity UBM/RDL Deposition by PVD for FOWLP Applications *Chris Jones, SPTS Technologies*	Ultra-thin Gold Passivation as a Viable Alternative for Achieving Low Temperature, Low Pressure Cu-Cu Thermocompression Bonding *Satish Bonam, Ph.D., IIT HYDERABAD*	Wafer-Level Vacuum-Packaged 2-Axes MEMS Gyroscope with High Yield Rate *ChungMo Yang, Ph.D., National Nano Fab Center*
4:45pm	Addressing the Needs of RDL/UBM Processing in FOWLP *Frantisek Balon, Ph.D., Evatec AG*	Electrodeposition of Ø50 × 50μm Cu Pillars for 3D Stacking Applications *Zaid El-Mekki, imec*	Photolithography Alignment Mark Transfer System for Low Cost Advanced Packaging and Bonded Wafer Applications *Keith Best, Rudolph Technologies*

	Thursday, October 20, 2016		
	7:30am Registration Opens		
Workshop#	**Instructor**	**Day/Time**	**Topic**
WS1	Beth Keser, Ph.D. Qualcomm	8:30am-12:00pm | Donner	Introduction to Fan-Out Wafer-Level Packaging
WS2	Chip Spangler, Ph.D. Aspen Microsystems, LLC	8:30am-12:00pm | Siskiyou	Wafer-Level Packaging for the Functional Integration of MEMS and ICs
WS3	Chet Palesko, SavanSys Solutions LLC and Jan Vardaman, TechSearch International, Inc.	1:30pm-5:00pm | Donner	Choosing the Right IC Packaging
WS4	John Lau, Ph.D. ASM Pacific Technology	1:30pm-5:00pm | Siskiyou	Recent Advances and New Trends in Semiconductor Packaging