Sessions at a Glance: Tuesday, October 13

7:00 AM	Registration Opens Bayshore Foyer		
	WLP TRACK | MONTEREY ROOM	3D TRACK | SAN CARLOS ROOM	MEMS TRACK | SANTA CLARA
	Session 1: Fan Out WLP Technologies and Applications	Session 2 - TSV Processing Considerations	Session 3 - MEMS and Sensor Packaging Solutions
8:30 AM	Fan-Out Wafer Level Packaging: Market and Technology Trends Thibault Buisson, Yole Développement	A Study of Microbump Metrology and Defectivity at 20um Pitch and Below for 3D TSV Stacking Maarten Liebens, IMEC	Full Hermetic 3D Wafer-Level-Packaging for LED and Sensor Modules Martin Wilke, P.Eng., Fraunhofer IZM
9:00 AM	Fan-Out WLP Technology as 2D, 3D System in Packaging (SiP) Solution Jong Heon Kim, Ph.D., Nepes Corporation	Methods for Assembly of TSV Products Tom Strothmann, Kulicke & Soffa	Advanced MEMS and Packaging: Photoresist, Adhesive and Thin Film Processing Solutions for Lift-Off Processing Richard Redburn, EV Group, and Steven Sorrentino, Materion
9:30 AM	Integration Through Wafer-Level Packaging Approach Kai Liu, Ph.D., STATS ChipPAC	Wet Cleaning as an Improved Final Quality Control of DRIE-Produced Features Travis Acra, Dynaloy LLC	SiP's for Internet of Things (Iot)– 3D CIS/IC and MEMS/IC Integration John Lau, Ph.D., ASM Pacific Technology
10:00 AM	TBA	3D Packaging & SiP Technology Technology Trends Hamid Eslampour, STATS ChipPAC	Scalable High-rate Nanoscale Printing for Electronics, Interconnects, Sensors, Energy and Materials Applications Ahmed Busnaina, Ph.D., Northeastern University
10:30 AM	Refreshment Break Exhibit Hall		
11:10 AM	Welcome Comments - Steven Xu, Ph.D., Qualcomm, Conference Chair OAK BALLROOM (2ND FLOOR)		
11:20 AM	Keynote Address: Rama Alapati, Director of GLOBALFOUNDRIES - Package Architecture & Customer Technology (PACT) High Density Fan-Out: Evolution or Revolution OAK BALLROOM (2ND FLOOR)		
12:15 PM	Lunch Break Exhibit Hall		
	WLP TRACK | MONTEREY ROOM	3D TRACK | SAN CARLOS ROOM	MEMS TRACK | SANTA CLARA
	Session 4 - Fan-Out WLCSP	Session 5 – 3D and TSV Metrology Methodologies	Session 6 - MEMS Process Technologies
1:45 PM	An Analysis of Key Cost and Yield Drivers for Fan-Out Wafer-Level Packaging Amy Palesko, SavanSys Solutions LLC	Metrology Considerations for Through Silicon Via Manufacturing Ke Xiao, Ph.D., Nanometrics, Inc	An Experimental Investigation on the Covering Process of the Polymer Chip with Various Geometries Jae Sung Yoon,Ph.D., Korea Institute of Machinery & Materials (KIMM)
2:15 PM	Temporary Wafer Carrier Solutions for Thin FOWLP and eWLB-based PoP Thomas Uhrmann, Ph.D.,EV Group and Jose Campos, NANIUM, S.A.	The X-Ray Metrology of TSV's David Bernard, Ph.D., Nordson DAGE	Improving Device Yields and Throughput Using Plasma Dicing Dave Thomas, Ph.D., SPTS Technologies
2:45 PM	Chips "Face-Up" Panelization Approach for Fan-Out Packaging Boyd Rogers, Ph.D. and Debbie Sanchez, Deca Technologies	Approaches and Challenges for 3D Packaging Charles Woychik, Ph.D., Invensas Corporation	3D-WLP by Using Cu-TSV for Thin MEMS Accelerometer Packages Lutz Hofmann, Fraunhofer ENAS
3:15 PM	Refreshment Break Exhibit Hall		
4:00 PM	Panel Discussion: Fan-Out WLP Panel Processing OAK BALLROOM (2nd FLOOR)		
	Moderator: Jan Vardaman, President, TechSearch International, Inc. Panelists: Jose Campos, NANIUM, S.A. Bill Chen, ASE Tim Olson, Deca Technologies Beth Keser, Ph.D., Qualcomm Thomas Uhrmann, Ph.D.,EV Group Curtis Zwenger, Amkor Technology		
5:30 PM	Exhibitor Reception Exhibit Hall		

Sessions at a Glance: Wednesday, October 14

7:00 AM	Registration Opens Bayshore Foyer		
8:30 AM	Keynote Address: Sitaram Arkalgud, VP of Invensas - 2.5D/3D IC,Examining Low Cost Alternatives OAK BALLROOM (2ND FLOOR)		
9:30 AM	Refreshment Break Exhibit Hall		
	WLP TRACK | MONTEREY ROOM	3D TRACK | SAN CARLOS ROOM	WLP TRACK | SANTA CLARA
	Session 7 - Fan-In WLP Advances	Session 8 - Emerging 2.5 and 3D Process Technologies	Session 9 - Cu Pillar Bumping and Assembly Considerations
10:15 AM	Fan-In WLP: Technology and Market Trends Andrej Ivankovic, Ph.D., Yole Développement	Interposer Based Integration of Advanced Memories and an ASIC Muhammed Waqas Chaudhary, Fraunhofer IIS/EAS	Assembly and Reliability Characterization of FCCSP with Fine Pitch Cu PIllar Bump on Thin Coreless Substrate Using No-Clean Flux and Molded Underfill Weidong Liu, Huatian Technology and Ted Tessier, FlipChip International
10:45 AM	Final Test Solution of WLCSP Devices Michael Frazier, Xcerra Corporation	Optimization of Through Si Via Last Lithography for 3D Packaging Gareth Kenyon, Ultratech Inc.	Assemblies Containing Copper Pillar Structures Processed Using One Step Chip Attach Materials (OSCA) and Conventional Mass Reflow Processing Daniel Duffy, Kester an ITW Company
11:15 AM	Dual Chip Wafer-Level CSP with Sintering Paste LGA Catherine Shearer, P.E.,Ormet Circuits, Inc.	Comparison Between Wet and Dry Si via Reveal in 3D Backside Processing Dave Thomas,Ph.D., SPTS Technologies	Low Cost Solutions for Cu Pillar Flip Chip Package Fernando Roa, Ph.D., Amkor Technology
11:45 AM	Development Approach & Process Optimization for Sidewall WLCSP Protection Lee Smith, UTAC	Structural Integrity of a 3D TSV Package Under Thermal Loading; Structural Mechanics Based Study Mohammed Shahid Ali, M.S., University of Texas at Arlington	Process Controls for Electroless Ni/Au Metallization Peter Bratin, Ph.D., ECI Technology
12:15 PM	Lunch Break Exhibit Hall		
1:45 PM	Panel Discussion: Interposers, 3D TSVs, and Alternatives: What are the Options and Where do They Fit? OAK BALLROOM (2nd FLOOR)		
	Moderator: Françoise Von Trapp, 3D InCites Panelists: Aric Shorey, Corning, Inc. Thibeault Buisson,Yole Développement Hughes Metras, CEA-Leti Mike Kelly, Amkor Technology		
3:15 PM	Refreshment Break Exhibit Hall		
	WLP TRACK | MONTEREY ROOM	3D TRACK | SAN CARLOS ROOM	WLP TRACK | SANTA CLARA
	Session 10 - WLP Process and Lithography	Session 11 - Thin 3D Enabling Technologies	Session 12 - Equipment Advances in WLP
4:00 PM	Advanced Lithography and Electroplating for High Aspect Ratio Cu Pillars Keith Best, Rudolph Technologies	Ultra-Thin Component Embedded Packaging using Polyimide-Based Platform Arun Gowda, Ph.D., GE Global Research	Massively Parallel 3D Inspection and Metrology of µFeatures in 3D Packaging Arun Aiyer, Ph.D. and Tianheng Wang, Ph.D., Frontier Semiconductor
4:30 PM	Cleaning Copper Pillar Flip Chip Die without Attack to Exposed Metals Mike Bixenman DBA, KYZEN Corporation	Thin Wafer 3D-TSV Processing Temporary Bonding Adhesive Film Fred Lo, Ph.D., and Kevin Chung, Ph.D., AI Technology, Inc.	DSC300 Gen2 Platform Combines Projection Lithography Performance with Advantages of Full-field Exposure Technology Habib Hichri, Ph.D., SUSS MicroTec
5:00 PM	Stencil Design for Wafer Level Ball Drop and Flip Chip Assembly Sue Holmes, Photo Stencil	A High Temperature Vapor Phase Polymer for Wafer-Level Packaging Rakesh Kumar, Ph.D., Specialty Coating Systems	Photolithography Study for High-Density Integration Technologies Hiromi Suda, Canon Inc.
5:30 PM	IWLPC Conclusion		