The European 3D Technology Platform for Heterogeneous Systems

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Performance and productivity of microelectronics have increased continuously over more then four decades due to the enormous advances in lithography and device technology. However, today it has become questionable if this so-called “More Moore” development alone will be able to overcome the predicted performance and cost problems of future IC fabrication. The ITRS roadmap predicts 3D integration as a key technology and corresponding solutions will most probably be based on through silicon via (TSV) technology. Many institutes and companies have demonstrated full 3D integration processes. A large percentage of the process flows that are demonstrated early on in a technological evolution are usually feasible but are not commercially viable. But which microelectronic products based on TSV technologies are at present actually in the market? CMOS image sensors using a “via last” approach with via diameters of about 50 µm and similar silicon thicknesses have been already introduced in the market mainly driven by form factor. In Europe STMicroelectronics developed a 2M pixel mobile-phone camera module VD6725 which is fabricated using TSV. The CMOS image sensor products are being fabricated in their Crolles facility.

3D stacking of DRAM and NAND memories by applying TSV technology is in development and has been reported to be technically viable by e. g. Samsung, Elpida and Micron. Chip-on-Chip (CoC) stacking of memory and logic devices without TSVs is already widely introduced in the market. Applying TSV technology for memory on logic will increase the performance of these advanced products and simultaneously shrink the form factor.

In addition to the enabling of further improvement of transistor integration densities (“More Moore”), 3D integration is a well-accepted approach for so-called “More than Moore” applications with their essential need for integration of heterogeneous technologies. Miniaturized MEMS/IC products represent a typical example for such heterogeneous systems demanding for smart system integration rather than extreme high transistor integration densities.

In Europe, many companies and research organizations are working currently in the area of 3D integration; several of them with a long-standing history and great expertise, as e. g. 3D-PLUS, Siemens, Infineon and Fraunhofer (since mid 1980´s). The European industry will benefit - from their strong background in microsystems technologies - of focusing on “More than Moore” products with their need of heterogeneous system integration: Heterogeneous combination of elements to integrate higher levels of intelligence into multifunctional microsystems including multisensing, processing, wireless and wired communication, and/or actuation capabilities. 3D integration is a very promising cost-effective approach for the realization of such heterogeneous systems.

The European 3D technology platform that has been established within the e-CUBES project is focusing on the requirements coming from heterogeneous systems. Seven corresponding technologies were successfully developed in all relevant categories of 3D Integration:

a) 3D System-on-Chip (3D-SOC): Fraunhofer´s post BEOL TSV Technology (ICV-SLID) and SINTEF´s Hollow Via & Gold Stud Bump Bonding (HoViGo),
b) 3D Wafer-Level Packaging (3D-WLP): IMEC / Fraunhofer´s Thin-Chip-Integration Technology (TCI/UTCS) and CEA-LETI´s Via Belt Technology, and
c) 3D System-in-Package (3D-SIP): 3D-PLUS´ High Performance Package-in-Package (HiPPiP) and Wireless Die-on-Die (WDoD) Technologies, as well as Tyndall´s Submicron Wire Anisotropic Conductive Film Technology (SW-ACF).

The 3D integration technologies which form part of the established e-CUBES platform will be presented including key characteristics, critical dimensions, electrical parameters and adaptability for future applications.