15th Annual

International Wafer-Level Packaging Conference & Exhibition

"DRIVING AN INTERCONNECTED WORLD"

October 23-25, 2018
San Jose, California, USA

www.iwlpc.com

Conference: October 23-24
Exhibits: October 23-24
Courses: October 25

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Welcome to the 15th Annual International Wafer-Level Packaging Conference!

IWLPC brings together the semiconductor industry's most respected authorities addressing all aspects of Wafer-Level Packaging, 3D and Advanced Manufacturing and Test.

Conference Chair
Curtis Zwenger, *Amkor Technology, Inc.*

Technical Chair
Chris Scanlan, *Deca Technologies, Inc.*

Executive Team
Tanya Martin, *SMTA*
Jenny Ng, CMP, *SMTA*
Lawrence Michaels, *Chip Scale Review*
Kim Newman, *Chip Scale Review*

3D Integration Track
Laurette Nacamulli, *Dow Chemical Co.,* Chair
Peter Ramm, Ph.D., *Fraunhofer EMFT,* Co-Chair
Arun Aiyer, Ph.D., *Rudolph Technologies*
Brian Bircumshaw, *exo-imaging*
Sam Gu, Ph.D., *Huawei R&D USA*
David Hiner, *Amkor Technology, Inc.*
John Lau, Ph.D., *ASM Pacific Technology*
Anup Pancholi, *Intel*
Herb Reiter, *eda 2 asic Consulting, Inc.*
Jeremy Theil, *XPERI/Invensas*
Dimitrios Velenis, *imec*
Seung Wook Yoon, Ph.D., MBA, *STATS ChipPAC*

Wafer-Level Packaging Track
Saurabh N. Athavale, Ph.D., *Maxim Integrated Products,* Chair
Tom Strothmann, *Kulicke & Soffa Industries,* Co-Chair
Vivek Dutta, Ph.D., *EMD Performance Chemicals*
Jie Gong, Ph.D., *KLA-Tencor*
Jan Vardaman, *TechSearch International, Inc.*
Marion Volpert, *CEA Leti*
Steven Xu, *Qualcomm*

Advanced Manufacturing and Test
Shekar Krishnaswamy, *Applied Materials,* Chair
Ira Feldman, *Feldman Engineering Corp.,* Co-Chair
Dale Gee
Habib Hichri, Ph.D., *SÜSS MicroTec Inc.*
Gerard John, *Amkor Technology*
John Lannon, Ph.D., *Micross Advanced Interconnect Technology LLC*
Subhasis Mukherjee, Ph.D., *SanDisk*
Garrett Oakes, *EV Group*

Join industry leaders, technologists and innovators at the 15th Annual International Wafer-Level Packaging Conference & Exhibition (IWLPC). Held in San Jose, CA, the IWLPC continues to be the premier semiconductor packaging conference and exhibition focused on wafer-level packaging. This year's conference theme, "Driving an Interconnected World," emphasizes the growing importance of advanced wafer-level interconnect technologies to enable advanced system-level packaging solutions for applications such as automotive, communications, and high-performance computing.

The IWLPC provides a dynamic environment for learning, networking and technical exchange. This year's conference comprises three major parts: the technical program, the courses, and the technology exhibition. The technical program has three parallel tracks with two full days of presentations on wafer-level packaging, 3D integration, and advanced manufacturing technologies. We'll be building on the success of last year's conference, which was recognized as the strongest IWLPC technical program to date.

IWLPC will also feature three keynote talks by leaders in the industry: Douglas C.H. Yu, Ph.D., TSMC ("Growth of WSI and Wafer Foundry with Moore's Law and More than Moore, and Vice Versa"); Walden Rhines, Ph.D., Mentor, a Siemens Business ("Monolithic vs. Heterogeneous Packaging: Where Does the Future Lie?"); and Veer Dhandapani, Ph.D., NXP Semiconductors ("Interconnected World and the Automotive Paradigm"). In addition, Jan Vardaman and Tanja Braun, Dr.-Ing., will moderate a panel discussion entitled, "What is the Sweet Spot for Large Area (Panel) Packaging?" Four Professional Development Courses will be offered. We look forward to seeing you this October in San Jose, California. Let's have another great IWLPC!

— Curtis Zwenger, *Amkor Technology, Inc.*
IWLPC General Chair

— Chris Scanlan, *Deca Technologies, Inc.*
IWLPC Technical Chair

The Conference and Exhibition is co-produced by the SMTA, the premier global organization for electronics assembly, and *Chip Scale Review*, the leading global industry publication for the semiconductor packaging community.

2018 IWLPC
15th International Wafer-Level Packaging Conference

"DRIVING AN INTERCONNECTED WORLD"

3D Integration Track

Since the mid 2010's, 3D integration technologies are well-accepted approaches for fabrication of high-performance memory-enhanced products, explicit stacked DRAMs, which are in high volume production at Samsung, Hynix and Micron. 3D integrated devices are today in most mobiles and so finally, after more than three decades of R&D, 3DIC Integration has arrived in the electronic industry! On the other hand, there is still no high volume memory-on-logic production. Major issue is the high cost of corresponding sophisticated 3DIC processes, but another reason for postponing the introduction of 3D memory-on-logic is the big success of TSV interposer technology. On top of the memory-enhanced product developments, industrial consortia have been targeting on 3D integration as a key technology for heterogeneous IC/MEMS products, demanding smart system integration rather than extreme high-interconnect densities (a.o. the European e-BRAINS platform). In general, heterogeneous integration technologies are being developed for functional diversification systems, for example, integration of CMOS with other devices, such as analog/RF, solid state lighting, HV power, passives, sensors/ actuators, chemical and biological sensors and bio-medical devices. This heterogeneous integration started with system-in-packaging technology, and is expected to evolve into 3D heterogeneous integration. Besides the application of TSV processes, the key technology in order to achieve high reliability is low temperature die/wafer bonding based on robust processes such as SLID/TLP, oxide-oxide and Cu/oxide hybrid bonding. Many R&D activities worldwide are focusing today on 3D heterogeneous integration for novel functionalities. The multitude of abstracts submitted to the 2018 IWLPC is evidence of the vast activities and interest on the subject matter. The 3D Integration sessions intend to bring you a sample of these advances in 3DIC, TSV interposer technology, 3D heterogeneous integration, temporary wafer bond (TWB) processing, among others.

Advanced Manufacturing and Test Track

The Advanced Manufacturing and Test Track is devoted to manufacturing challenges and solutions. Wafer level packaging (WLP) and many other advanced packaging technologies are now in high-volume manufacturing (HVM) wherein the productivity challenges are different from the challenges of research and development (R&D). Through innovation, integrated circuit (IC) manufacturers and equipment manufacturers have been able to overcome many of these challenges as new packaging technologies have been commercialized as new products have been introduced. This track will showcase these solutions which have been categorized into the following sessions: process and equipment improvements, new methods and materials, and measurement and test strategies. Attendees to the presentations in this track will benefit from the experiences and solutions shared by end-customers and manufacturers alike.

WLP Track

Wafer-Level Packaging (WLP) in its standard form has been a commonly used package in many applications ranging from handheld mobile to telecom, owing to its form and cost factor. Due to WLP's virtues of simplicity, high performance and adaptability – industry is pushing the WLP envelope further with latest development in the field of Fan Out WLP. This track covers IWLPC theme and industry trend by focusing on key areas of development in Reliability, Packaging, Process & Metrology and Scaling (Manufacturing).

Professional Development Courses

On Thursday, October 25, we will have professional development courses given by instructors who are pre-eminent authorities in their fields. Each course represents an outstanding opportunity to meet with your peers in a relaxed atmosphere for an intensive course mentored by an expert.

Exhibition

On October 23-24, the IWLPC will present more than 60 exhibiting companies-many which are the leaders in the semiconductor packaging and test industry. Attendees will be able to see the latest products and discuss a broad range of services in an interactive environment.

The International Wafer-Level Packaging Conference has become one of the premier forums focused in three key technology areas: Wafer-Level Packaging, 3D and Advanced Manufacturing and Test.

SESSIONS AT A GLANCE:
Tuesday, October 23

Time	Program		
7:00am	**REGISTRATION OPENS**		
8:00am	**CONTINENTAL BREAKFAST** – Bayshore Ballroom		
8:45am	**OPENING COMMENTS –** Oak Ballroom (2nd Floor) Conference Chair: Curtis Zwenger, *Amkor Technology, Inc.*		
9:00am	**KEYNOTE ADDRESS: Growth of WLSI and Wafer Foundry with Moore's Law and More-Than-Moore and Vice Versa** Douglas C.H. Yu, Ph.D., Vice President, Research & Development, *Taiwan Semiconductor Manufacturing Company (TSMC)*		
10:00am	**REFRESHMENT BREAK** Exhibit Hall		
	WLP Track **10:30am-12:30pm (Oak)** **Session 1: Package Reliability and Performance**	**3D Track** **10:30am-12:30pm (Pine)** **Session 2: Processing Technologies**	**Advanced Manufacturing and Test Track** **10:30am-12:30pm (Cedar)** **Session 3: Design & Characterization**
10:30am	**Board Level Reliability Study of Next Generation Large Die Wafer Level Chip Scale Package Structures** Timo Henttonen, *Microsoft*	**Models for Improved Electroplating of TSV in 3DIC** Sridhar Narayanaswamy, Ph.D. *Institute of High Performance Computing*	**Test Methods and Parameters to Interpret Wafer Level Packaging's Workability and Reliability** SeungYong Yang, *Samsung SDI*
11:00am	**Chip Board Interaction Analysis of 22FDX® Wafer Level Packaging and its Potential for System in Package Applications** Jae Cho, *GlobalFoundries*	**Wave Front Phase Imaging of Wafer Warpage** Jan Gaudestad, *Wooptix*	**A Practical Guide for First-Time FOWLP Design Success** Keith Felton *Mentor, a Siemens Business*
11:30am	**An Innovative Application of Fan-Out Packaging for Test & Measurement-Grade Products** Barrett Poe, *Keysight Technologies*	**High Density and High Bandwidth Chip-to-chip Connections with 20µm Pitch Flip-chip on Fan-Out Wafer Level** Arnita Podpod, *imec*	**High Speed 3D Inspection of Advanced Package Interconnect Uniformity** John Schaefer, *Rudolph Technologies*
12:00pm	**Wafer-Level Fan-Out for High-Performance, Low-Cost Packaging of Monolithic RF MEMS/CMOS** Rameen Hadizadeh, *WiSpry*	**Fabrication of a High Precision Magnetic Position Sensor based on a Through Silicon Via First Approach** Zai Zoschke, *Fraunhofer IZM*	**Design Trends and Challenges of Advanced Wafer-Level Manufacturing and Fanout** Bill Acito, *Cadence Design Systems*
12:30pm	**LUNCH BREAK**		
1:45pm	**KEYNOTE ADDRESS: Monolithic versus Heterogeneous Packaging: Where Does the Future Lie?** Walden Rhines, Ph.D., President and Chief Executive Officer, *Mentor, a Siemens Business*		
	WLP Track **3:00pm-4:30pm (Oak)** **Session 4: Advancements in WLP Integration Technology**	**3D Track** **3:00pm-4:30pm (Pine)** **Session 5: Advanced Technologies**	**Advanced Manufacturing and Test Track** **3:00pm-4:30pm (Cedar)** **Session 6: New Methods & Materials**
3:00pm	**Advanced Packaging Fabrications and Die Assembly for Large Surface Interconnects** Nohora Caicedo, *CEA Leti*	**Advanced RF Packaging Technology Trends, from WLP to 3D integration toward 5G and mmWave Application** Stéphane Elisabeth, Ph.D. *System Plus Consulting*	**Advancing Advanced Process Control in Backend Factories** Ben Williams, *Applied Materials*
3:30pm	**Fan-Out Wafer Processing in the High Density Packaging Era** David Butler, *SPTS Technologies Ltd.*	**Antenna Integration Technologies for 5G Car-application** Andy Heining, *Fraunhofer, EAS*	**Market Trend of Temporary Wafer Bonding Solution as an Enabler in Advanced Packaging** Jay (Ji) Cheng, Ph.D., *Intel Corporation*
4:00pm	**Heterogeneous Integration Challenges within Wafer Level Fan-Out SiP for Wearables and IoT** Eoin O'Toole, *Amkor Technology Portugal, S.A.*	**Comparative Study of 3D Package Configurations in Power Delivery and Thermal Perspective** Heeseok Lee, *Samsung Electronics*	**Fine RDL Formation Using Alternative Patterning Solution for Advanced Packaging** Habib Hichri, Ph.D., *SÜSS MicroTec Inc.*
4:30pm	**NETWORKING RECEPTION**		
6:00pm	**ADJOURN**		

SESSIONS AT A GLANCE:

Wednesday, October 24

Time	WLP Track	3D Track	Advanced Manufacturing and Test Track
7:00am	REGISTRATION OPENS		
8:00am	CONTINENTAL BREAKFAST – Bayshore Ballroom		
9:00am	**KEYNOTE ADDRESS: Interconnected World and the Automotive Paradigm** Veer Dhandapani, Ph.D., Head of Automotive Packaging, *NXP Semiconductors*		
10:00am	REFRESHMENT BREAK Exhibit Hall		
	WLP Track 10:30am-12:30pm (Oak) Session 7: Wafer Level Fan-Out Process & Metrology	**3D Track** 10:30am-12:30pm (Pine) Session 8: Processing & Materials	**Advanced Manufacturing and Test Track** 10:30am-12:30pm (Cedar) Session 9: Process & Technology
10:30am	**Advanced Packaging Metrology and Lithography that Overcomes FOWLP/ FOPLP Die Placement Error** Keith Best and Mike Marshall *Rudolph Technologies*	**Improve Control Amidst Die Shrink, 3D Package Complications** Matt Wilson, *Rudolph Technologies*	**Thermal Debonding and Warpage Adjust of FOWLP – A Crucial Step in the Evolution of Advanced Packaging?** Klemens Reitinger, *ERS*
11:00am	**Optical Run-Out Correction for Improved Lithography Overlay Accuracy for FOWLP Applications** Markus Arendt *SUSS MicroTec Photonic Systems Inc.*	**Reducing the Cost of Applying Ultra-Thin, Package Level EMI Shield Coatings** Stuart Erickson, *Ultrasonic Systems, Inc.*	**Degas Module Thermal Architecture, Variable Wafer Delays, and Throughput, Productivity, and Consistency in Fan-Out Packaging Barrier/Seed Layer PVD** Paul Werbaneth, *Intevac, Inc.*
11:30am	**The Effective Solution for Wafer-Level Package Warpage Control by Low Temp Curable WLP Granule & Powder Encapsulation Materials** Junghwa Kim, *Samsung SDI*	**Plasma Deposited Hydrophobic Silicone Multilayer Polymeric Coating** Abe Ghanbari, *Semblant*	**Significant Advancement in Laser Ablative Release Layer Material Design Enabling Low-Energy and Low-Residue Debond** Luke Prenger, *Brewer Science*
12:00pm	**Exposed Die Fan-Out Wafer Level Packaging by Transfer Molding** Henk Wensink, *BESI Netherlands BV*	**Enabling Reliability of 3D TSV Advanced Packages with Non-Conducive, Pre-Applied Underfill Film Material** Jie Bai, Ph.D., *Henkel Electronics Materials*	**Failure Relief in FOWLP Polymer Layers** Robert Hubbard, Ph.D., *Lambda Technologies, Inc.*
12:30pm	LUNCH BREAK		
	WLP Track 1:30pm-3:30pm (Oak) Session 10: Panel Level Fan-Out Packaging	**3D Track** 1:30pm-3:30pm (Pine) Session 11: Wafer Bonding Applications	**Advanced Manufacturing and Test Track** 1:30pm-3:30pm (Cedar) Session 12: Process & Technology II
1:30pm	**Recent Developments in Panel Level Packaging** Tanja Braun, Dr.-Ing., *Fraunhofer IZM*	**Development of Low Temperature Direct Bond Interconnect Technology for Die-to-Wafer and Die-to-Die Applications – Stacking, Yield Improvement, Reliability Assessment** Guilian Gao, Ph.D., *XPERI/Invensas*	**Spin vs. Spray Coating Techniques for Advanced Packaging** Sai Sarath Reddy Kamana *Rochester Institute of Technology*
2:00pm	**Fabrication of Redistribution Structure Using Highly Reliable Photosensitive Polyimide for Fan Out Panel Level Packages** Hitoshi Araki, Ph.D., *Toray Industries*	**Temporary Bonding and the Challenge of Cleaning Post Debond** Laura Maurer *Veeco Precision Surface Processing*	**The Road to Wafer-On-Wafer (WOW) High Volume Manufacturing (HVM)** Boris Kesil, *Quartet Mechanics*
2:30pm	**Overcoming Critical Scaling Challenges in Fine Line RDL Lithography and Plating Processes at Panel Scale** Robert Moon, *TEL NEXX*	**The Development of a Thermo Compression Flip Chip Bonding Process Optimized for 3D Die Stacking** Dev Gupta, *APSTL*	**An Effective Method to Improve Productivity Performance** Quor Hahn Leong, *Applied Materials*
3:00pm	**Study of Fine Pitch RDL First FO-PLP/WLP** Keisuke Nishido, *Hitachi Chemical*	**Collective Bonding for Heterogeneous Integration in Advanced Packaging** Thomas Uhrmann, *EV Group*	**Advanced eWLB (embedded Wafer Level Ball Grid Array) Solutions for mmWave Applications** SW Yoon, *STATS ChipPAC*
3:30pm	NETWORKING BREAK Exhibit Hall		
4:00pm	**PANEL DISCUSSION: What is the Sweet Spot for Large Area (Panel) Packaging?** Moderators: E. Jan Vardaman, *TechSearch International, Inc.* Tanja Braun, Dr.-Ing., *Fraunhofer IZM*		
5:00pm	CLOSING COMMENTS		

Professional Development Courses 7:30am REGISTRATION OPENS

Course#	Instructor	Day/Time	Topic
PDC1	John Hunt, *ASE*	Thursday, October 25 8:30am-12:00pm	Fan Out Packaging Technology Evolution
PDC2	Gil Sharon, *DfR Solutions*	Thursday, October 25 8:30am-12:00pm	Modeling Failure Modes for Chip Package Interactions and Package Level Reliability
PDC3	John Lau, *ASM*	Thursday, October 25 1:30pm-5:00pm	Fan-Out Wafer/Panel-Level Packaging for 3D IC Heterogeneous Integration
PDC4	Jeffrey Gotro, Ph.D., *InnoCentrix, LLC*	Thursday, October 25 1:30pm-5:00pm	Polymers and Processes Used in Wafer Level Packaging

Thursday, October 25

8:30am-12:00pm | San Carlos Room

PDC1

Fan Out Packaging Technology Evolution

John Hunt, *ASE*

Overview

This course will review how the integration of a wide variety of packaging technologies, wafer level processing, substrate evolution and Flip Chip packaging structures have come together into 2D and 3D Fan Out packages. It will further explore the higher levels of integration and sophistication using Fan Out as a basic manufacturing technology, describing the evolving functionality and complexity achieved by combining low cost materials and innovative process flows. By using such combinations of tools and processes, the resulting packages are evolving into increasingly complex structures for both low density mobile and higher density server applications.

Who Should Attend?

Engineers, managers, and purchasing individuals who want to understand the basics and variety of options available using Fan Out packaging technologies.

8:30am-12:00pm | San Martin Room

PDC2

Modeling Failure Modes for Chip Package Interactions and Package Level Reliability

Gil Sharon, *DfR Solutions*

Overview

This course will cover prediction methodologies for flip chip die and package level reliability. The mechanical process for several failure modes will be discussed with examples of die cracking, bump fatigue, white bump, package warpage, board level reliability and microvia failures. Modeling methodologies for each of the failure modes will be shown. Possible mitigation strategies and options at the package level will be explored. The physical and mechanical processes of attaining reliability are an integral part of this course. Participants are expected to have a basic knowledge of BGA, QFN and Package-on-Package structures. Participants should also be familiar with finite element modeling and analysis methods.

Who Should Attend?

This course is directed towards the fabless semiconductor manufacturing segment. Participants should be involved in design, manufacturing or purchasing of flip chip packaging services. This course will be especially helpful to device manufacturers and designers.

1:30pm-5:00pm | San Carlos Room

PDC3

Fan-Out Wafer/Panel-Level Packaging for 3D IC Heterogeneous Integration

John Lau, Ph.D., *ASM Pacific Technology*

Overview

Because of the drive of Moore's law, SoC (system-on-chip) has been very popular in the past 10+ years. Unfortunately, the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC. Heterogeneous integration contrasts with SoC. Heterogeneous integration uses packaging technology to integrate dissimilar chips with different functions into a system or subsystem. For the next few years, we will see more implementations of a higher level of heterogeneous integration, whether it is for time-to-market, performance, form factor, power consumption or cost. Fan-out wafer-level packaging (FOWLP) has been getting lots of tractions since TSMC used their FOWLP to package the application processor for the iPhone 7. In this lecture, the following topics will be presented and discussed. Emphasis is placed on the latest developments of these areas in the past three years. Their future trends will also be explored.

Who Should Attend?

Students, engineers, and managers involved with any aspect of the electronics and optoelectronic industry, you should attend this course. It is equally suited for R&D professionals and scientists.

1:30pm-5:00pm | San Martin Room

PDC4

Polymers and Processes Used in Wafer Level Packaging

Jeffrey Gotro, Ph.D., *InnoCentrix, LLC*

Overview

The course will provide an overview of polymers and the important structure-property-process-performance relationships for polymers used in wafer level packaging. The main learning objectives will be: 1) understand the types of polymers used in wafer level packages, including underfills (pre-applied and wafer applied), mold compounds, and substrate materials 2) gain insights on how polymers are used in Fan Out Wafer Level Packaging, specifically mold compounds and polymer redistribution layers (RDL) 3) learn the key polymer and processes challenges in Fan Out Wafer Level Packaging.

Who Should Attend?

Packaging engineers involved in the development, production, and reliability testing of electronic packages would benefit. Those interested in gaining an understanding of the role of polymers and polymer-based processes used in wafer level packaging will also find this short course valuable.

Visit

www.iwlpc.com

to register today!

Special Events

Tuesday, October 23

Keynote Address
Growth of WLSI and Wafer Foundry with Moore's Law and More-Than-Moore, and Vice Versa

9:00am-10:00am, Oak Ballroom

Douglas Yu, Ph.D.
Vice President, Research & Development
Taiwan Semiconductor Manufacturing Company (TSMC)

Overview

Douglas C.H. Yu is a Vice President of TSMC R&D in charge of advanced interconnect and packaging technology development. He pioneered and delivered WLSI (Wafer-Level-System-Integration) technology platform, which includes 3DIC/TSV (CoWoS®), Integrated Fan Out Wafer-Level-Packaging (InFO) and advanced WL-CSP, for system integration of wide range products. Prior to that, Doug was responsible for the development and of industry's first advanced on-chip Cu/Low-K interconnects at TSMC's 0.13 micron technology node. He received Ph.D. degree on Materials Science and Technology from Georgia Institute of Technology. He has numerous publications and granted more than 500 US patents. Doug is an IEEE Fellow.

Keynote Address
Monolithic versus Heterogeneous Packaging: Where Does the Future Lie?

1:45pm-2:45pm, Oak Ballroom

Walden Rhines, Ph.D.
CEO & President
Mentor, a Siemens Business

Overview

Cost, risk, and the limitations of monolithic scaling are driving the growth of multi-die (heterogeneous) advanced IC packaging solutions. The integration of different functions into a highly optimized, yet variant-capable device is attractive to markets such as automotive, industrial IoT, and aerospace & defense, whose applications often do not have the quantities to justify the cost of a SoC implementation. Although system-in-package (SiP) has been around for some years and is well proven, the advent of high-density advanced packaging (HDAP) designs has stimulated the development of new tools and processes that can address such verification challenges as overall device connectivity, timing, functional verification, and thermal/stress analysis.

Wednesday, October 24

Keynote Address
Interconnected World and the Automotive Paradigm

9:00am-10:00am, Oak Ballroom

Veer Dhandapani, Ph.D.
Head of Automotive Packaging
NXP Semiconductors

Overview

Innovations in the automotive industry today are synonymous with technological advances not only in automotive domains such as electric power, braking etc. but also in mobile, home, office electronics and their applications to the automobiles we drive. Energy efficiency, the seamless connected car and advanced driver assist systems are the dominant trends driving the integration of highly innovative electronics in cars. This presentation will discuss how these technologies merge to serve the pilots of these advanced machines and the unique challenges that unifying these diverse domains provide. Meeting reliability, vehicle and functional safety as well as security requirements that the above trends dictate will be the focus of this presentation. These challenges are constantly evolving, especially as automotive electronics take advantage of the benefits of silicon scaling and incorporate leading edge nodes earlier than ever before. NXP Semiconductors, as the #1 Global Automotive supplier, is ideally poised to understand the needs of the automotive market and produce innovations with collaborative partners and suppliers. In addition to discussing the challenges, some of the unique solutions that NXP offers will also be discussed.

Panel Discussion
What is the Sweet Spot for Large Area (Panel) Packaging?

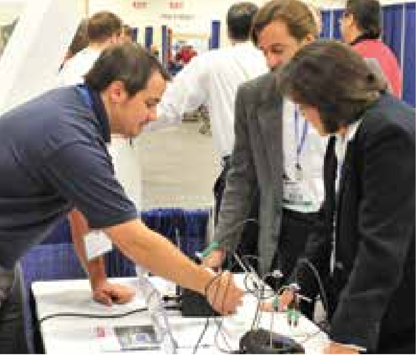
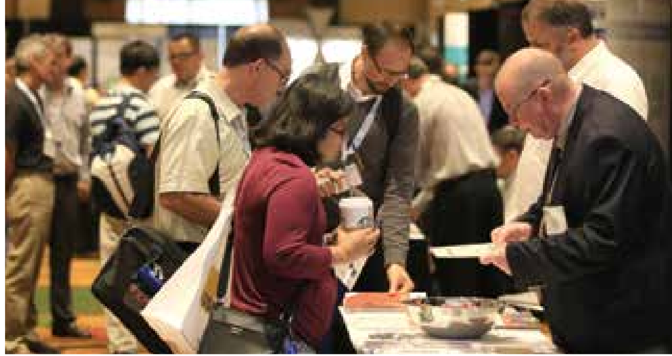
4:00pm-5:00pm, Oak Ballroom

Moderators: E. Jan Vardaman
President and Founder
TechSearch International, Inc.

Tanja Braun, Dr.-Ing.
Head of Group AET
Fraunhofer IZM

Overview

Fan-out Wafer Level Packaging has found widespread use in applications ranging from automotive and high-performance systems to mobile and consumer applications. A multitude of formats have been developed and moved into production. As with any package format, there is a quest for lower cost, and FO-WLP is no exception. Panel-level options are measured against wafer-level packaging and yield achievements. Until now the sweet spot for PLP is not really defined concerning target applications, integration density, panel size, lines and spaces, number of layers and yield. The topic on the sweet spot for PLP will be discussed with key players from the industry.

2018 Exhibition October 23 & 24

Four Reasons Your Company Should Exhibit at IWLPC!

1. Reach a focused international audience
2. Generate exposure in this highly competitive marketplace
3. Share new products and concepts in the market
4. Enhance relationships with existing customers and generate new leads

Exhibition:

Tuesday, October 23 | 10:00am-4:30pm
Wednesday, October 24 | 10:00am-4:00pm

Exhibition Reception:

Tuesday, October 23 | 4:30pm-6:00pm

What's Included:

- 8'x10' Pipe & Draped Booth or 6' Table Top
- Complimentary Lunch Each Day
- Refreshment Breaks
- Networking Reception
- Show Directory Listing
- Company Sign
- IWLPC Electronic Proceedings
- One Conference Pass (a $700 value)

Cost:

8'x10' Booth: $1,700
6' Table Top: $1,300

Don't miss your chance to exhibit, sells out early each year!

Attend the Exhibition for FREE!

- **Enjoy FREE refreshments and one-on-one networking with the industry's premier supplier companies.**
- **You don't need a conference pass to attend the exhibition, register online today!**

Register at www.iwlpc.com

Interested in exhibiting?

Visit www.iwlpc.com and click on Exhibitor Info Tab.

2018 IWLPC Exhibitors

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Registration & Pricing

Technical Conference Package

Your $700 conference fee includes: Technical Sessions, Proceedings, Exhibits and Reception Access, and Lunch each day. Register early to receive discounted pricing.

Single Day Registration

Your $450 fee includes all sessions of your choice on Tuesday, October 23 or Wednesday, October 24, exhibits, lunch and proceedings.

Courses

There will be one day of Professional Development Courses conducted by several of the most respected individuals in their fields. The fee of $250 includes one half-day course, handout materials and refreshments during breaks.

Proceedings

Proceedings are complimentary with one-or two-day registrations. The cost for additional proceedings is $300. Proceedings to be sent electronically.

Send Four, Pay for Three!

Your company can save over $700 by sending four attendees to the IWLPC. All registrants must be from the same company and must register at the same time. These rates are not available online. Contact Jenny Ng at 952-920-7682 and save!

Cancellations

If for any reason you should need to cancel a registration, there will be a $100 processing fee if received by September 28. After September 28, all registrations are final and refunds will not be issued; you may transfer your registration to a colleague. All requests must be in writing.

Early Registration Discount

The full conference, single day and course registration fees will increase by $100 after **September 28**. Register early to take advantage of the discount. This discount may not be combined with the student discount.

Discounted Hotel Rates

The IWLPC has made arrangements with our host hotel, the DoubleTree San Jose, to reserve a block of rooms for conference attendees at a special rate of only $229/night. Reservations must be made before September 28. We recommend booking early as the room block is expected to sell out. Please reference IWLPC to receive these rates. The hotel's phone number is 1-408-437-2186.

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15th Annual

International Wafer-Level Packaging Conference & Exhibition

October 23-25, 2018 DoubleTree Hotel, San Jose, CA USA

Conference: October 23-24 Exhibits: October 23-24 Courses: October 25

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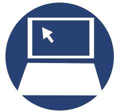

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- O *Tabletop Exhibition Attendee . . . . Free*
- O *Technical Conference Package $700*
- O *Technical Conference Speaker Rate $400*
- O *Technical Conference, Tuesday Only $450*
- O *Technical Conference, Wednesday Only $450*
- O *PDC1: Fan Out Packaging Technology Evolution $250*
- O *PDC2: Modeling Failure Modes for Chip Package Interactions and Package Level Reliability $250*
- O *PDC3: Fan-Out Wafer/Panel-Level Packaging for 3D IC Heterogeneous Integration. $250*
- O *PDC4: Polymers and Processes Used in Wafer Level Packaging $250*
- O *Conference Proceedings (sent electronically) $300*

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