2018 IWLPC Program

Tuesday, October 23

Time	WLP Track	3D Track	Advanced Manufacturing Track
7:00 AM	REGISTRATION OPENS		
8:00 AM	Coffee Networking		
8:45 AM	OPENING COMMENTS		
9:00 AM	**KEYNOTE: Growth of WLSI and Wafer Foundry with Moore's Law and More-Than-Moore and Vice Versa** *Douglas Yu, Taiwan Semiconductor Manufacturing Company (TSMC)*		
10:00 AM	BREAK IN THE EXHIBIT HALL		
	WLP Track (Oak)	3D Track (Pine)	Advanced Manufacturing Track (Cedar)
	Session 1: Package Reliability and Performance Chair: Saurabh Athavale Co-Chair: Ashok Pachamuthu	Session 2: Processing Technologies Chair: Arun Aiyer Co-Chair: John Duan	Session 3: Design & Characterization Chair: Andrei Berar Co-Chair: John Lannon
10:30 AM	Board Level Reliability Study of Next Generation Large Die Wafer Level Chip Scale Package Structures *Timo Henttonen, Microsoft*	Models for Improved Electroplating of TSV in 3DIC *Sridhar Narayanaswamy, Ph.D.* *Institute of High Performance Computing*	Challenges that the Semicon Industry gives X-Ray Technology and How we are working to Overcome them Keith Bryant, Yxlon International
11:00 AM	Chip Board Interaction Analysis of 22-NM Depleted Silicon on Insultator (FD-SOI) Technology in Wafer Level Packaging (WLP) *Jae Cho, Ph.D., GlobalFoundries*	Wave Front Phase Imaging of Wafer Warpage *Jan Gaudestad, Wooptix*	A Practical Guide for First-Time FOWLP Design Success *Keith Felton, Mentor, a Siemens Business*
11:30 AM	An Innovative Application of Fan-Out Packaging for Test & Measurement-Grade Products *Barrett Poe, Keysight Technologies*	High Density and High Bandwidth Chip-to-Chip Connections with 20µm pitch Flip-chip on Fan-Out Wafer-Level Package *Arnita Podpod, imec*	High Speed 3D Inspection of Advanced Package Interconnect Uniformity *Zonghu He, Rudolph Technologies*
12:00 PM	Wafer-Level Fan-Out for High-Performance, Low-Cost Packaging of Monolithic RF MEMS/CMOS *Rameen Hadizadeh, WiSpry*	Fabrication of a High Precision Magnetic Position Sensor based on a Through Silicon Via First Approach *Kai Zoschke, Fraunhofer IZM*	Design Trends and Challenges of Advanced Wafer-Level Manufacturing and Fanout *Bill Acito, IC Packaging Design Product Engineer* *Cadence Design Systems*
12:30 PM	LUNCH		
1:45 PM	KEYNOTE 2: **Discontinuities Drive Data Integration** Walden Rhines, Ph.D., Mentor, a Siemens Business		
	WLP Track	3D Track	Advanced Manufacturing Track
	Session 4: Advancements in WLP Integration Technology Chair: Tom Strothmann Co-Chair: Bora Baloglu	Session 5: Advanced Technologies Chair: Andy Heinig Co-Chair: Herb Reiter	Session 6: New Methods & Materials Chair: Garrett Oakes Co-Chair: Dale Gee
3:00 PM	Advanced eWLB (embedded Wafer Level Ball Grid Array) Solutions for mmWave Applications *Jacinta Aman Lim, STATS ChipPAC*	Advanced RF Packaging Technology Tends, from WLP to 3D integration toward 5G and mmWave Application *Stéphane Elisabeth,Ph.D., System Plus Consulting*	Advancing Advanced Process Control in Backend Factories *Ben Williams, Applied Materials*
3:30 PM	Fan-out Wafer Processing in the High Density Packaging Era *David Butler, SPTS Technologies Ltd*	Antenna Integration Technologies for 5G Car-Application *Andy Heinig, Fraunhofer EAS*	Laser-Assisted Bonding and Debonding *Dirk Müller, Ph.D., Coherent*
4:00 PM	Heterogeneous Integration Challenges within Wafer Level Fan-Out SiP for Wearables and IoT *Eoin O'Toole, Amkor Technology Portugal, S.A*	Comparative Study of 3D Package Configurations in Power Delivery and Thermal Perspective *Heeseok Lee, Samsung Electronics*	Fine RDL Formation Using Alternative Patterning Solution for Advanced Packaging *Habib Hichri, Ph.D., SÜSS MicroTec Inc.*
4:30PM-6:00PM	NETWORKING RECEPTION		

Wednesday, October 24

Time	WLP Track (Oak)	3D Track (Pine)	Test Track (Cedar)
7:00 AM	REGISTRATION OPENS		
8:00 AM	CONTINENTAL BREAKFAST		
9:00 AM	**KEYNOTE: Interconnected World and the Automotive Paradigm** *Veer Dhandapani, Ph.D., NXP Semiconductors*		
10:00 AM	BREAK IN THE EXHIBIT HALL		
	WLP Track (Oak)	3D Track (Pine)	Test Track (Cedar)
	Session 7: Wafer Level Fan-Out Process & Metrology Chair: Tom Strothmann Co-Chair: Marion Volpert	Session 8: Processing & Materials Chair: John Duan Co-Chair: Akash Agrawal	Session 9: Process & Technology Chair: Dale Gee Co-Chair: Garrett Oakes
10:30 AM	Advanced Packaging Metrology and Lithography that Overcomes FOWLP/FOPLP Die Placement Error *Keith Best and Mike Marshall, Rudolph Technologies*	Improve Control amidst Die Shrink, 3D Package Complications Woo Young Han, P.E., Rudolph Technologies	Thermal Debonding and Warpage Adjust of FOWLP – a Crucial Step in the Evolution of Advanced Packaging? *Klemens Reitinger, ERS*
11:00 AM	Optical Run-Out Correction for Improved Lithography Overlay Accuracy for FOWLP Applications *Markus Arendt, SUSS MicroTec Photonic Systems Inc.*	Reducing the Cost of Applying Ultra-Thin, Package Level EMI Shield Coatings *Stuart Erickson, Ultrasonic Systems, Inc.*	Degas Module Thermal Architecture, Variable Wafer Delays, and Throughput, Productivity, and Consistency in Fan-Out Packaging *Barrier/Seed Layer PVD* *Paul Werbaneth, Intevac, Inc.*
11:30 AM	The Effective Solution for Wafer-Level Package Warpage Control by Low Temp Curable WLP Granule & Powder Encapsulation Materials *Junghwa Kim, Samsung SDI*	Plasma Coating and Protection of Wearable Devices *Simon McElrea, Semblant*	Significant Advancement in Laser Ablative Release Layer Material Design Enabling Low-Energy and Low-Residue Debond *Luke Prenger, Brewer Science*
12:00 PM	Exposed die Fan-Out Wafer Level Packaging by Transfer Molding *Wilfred Gal, Besi Netherlands B.V.*	Enabling Reliability of 3D TSV Advanced Packages with Non-Conducive, Pre-Applied Underfill Film Material *Jie Bai, Ph.D., Henkel Electronic Materials*	Failure Relief in FOWLP Polymer Layers *Robert Hubbard, Ph.D., Lambda Technologies, Inc.*
12:30 PM	LUNCH		
	WLP Track	3D Track	
	Session 10: Panel Level Fan-Out Packaging Chair: Marion Volpert Co-Chair: Jan Vardaman	Session 11: Wafer Bonding Applications Chair: Anup Pancholi Co-Chair : Akash Agrawal	
1:30 PM	Recent Developments in Panel Level Packaging *Tanja Braun, Dr.-Ing, Fraunhofer IZM*	Development of Low Temperature Direct Bond Interconnect Technology for Die- to-Wafer and Die-to-Die Applications—Stacking, Yield Improvement, Reliability Assessment *Guilian Gao, Ph.D., XPERI/Invensas*	
2:00 PM	Fabrication of Redistribution Structure Using Highly Reliable Photosensitive Polyimide for Fan Out Panel Level Packages *Hitoshi Araki, Ph.D., Toray Industries*	Temporary Bonding and the Challenge of Cleaning Post Debond *Kenji Nulman, Veeco Instruments*	
2:30 PM	Redistribution-Layers (RDLs) for Fan-Out Panel-Level Packaging John Lau, Ph.D., ASM	Collective Bonding for Heterogeneous Integration in Advanced Packaging Thomas Uhrmann, Ph.D., EV Group	
3:00 PM	Study of Fine Pitch RDL first FO-PLP/WLP *Hitoshi Onozeki, Hitachi Chemical*	The Road to Wafer-On-Wafer (WOW) High Volume Manufacturing (HVM) *Boris Kesil, Quartet Mechanics, Inc.*	
3:30 PM	BREAK IN EXHIBIT HALL		
4:00 PM	**PANEL DISCUSSION: What is the Sweet Spot for Large Area (Panel) Packaging** Moderators: Jan Vardaman, TechSearch International, Inc. & Tanja Braun, Dr.-Ing., Fraunhofer IZM Richard Bae, Samsung Electro-Mechanics Company (SEMCO) Thomas DeBonis, Intel John Hunt, ASE Markus Leitgeb, AT&S Tim Olson, Deca Technologies		
5:00 PM	Closing Comments		

Thursday, October 25

	Professional Development Courses	
	Donner Pass Ballroom	Siskiyou Ballroom
8:30 AM	PDC1: Fan Out Packaging - Technology Evolution John Hunt, *ASE (US) Inc.*	PDC2: Modeling Failure Modes for Chip package Interactions and Package Level Reliability Gil Sharon, *DfR Solutions*

1:30 PM	PDC3: Fan-Out Wafer/Panel-Level Packaging for 3D IC Heterogeneous Integration John Lau, Ph.D., *ASM Pacific Technology*	PDC4: Polymers and Processes Used in Wafer Level Packaging Jeffrey Gotro, Ph.D., *InnoCentrix, LLC*