

## 2018 IWLPC Program

**Tuesday, October 23**

7:00 AM	REGISTRATION OPENS		
8:00 AM	CONTINENTAL BREAKFAST		
8:45 AM	OPENING COMMENTS		
9:00 AM	<p style="text-align: center;"><b>KEYNOTE: Growth of WLSI and Wafer Foundry with Moore's Law and More-Than-Moore and Vice Versa</b>  <i>Douglas Yu, Taiwan Semiconductor Manufacturing Company (TSMC)</i></p>		
10:00 AM	BREAK IN THE EXHIBIT HALL		
	WLP Track (Oak)	3D Track (Pine)	Advanced Manufacturing Track (Cedar)
	Session 1: Package Reliability and Performance Chair: Saurabh Athavale Co-Chair: Ashok Pachamuthu	Session 2: Processing Technologies Chair: Arun Aiyyer Co-Chair: John Duan	Session 3: Design & Characterization Chair: Andrei Berar Co-Chair: John Lannon
10:30 AM	Board Level Reliability Study of Next Generation Large Die Wafer Level Chip Scale Package Structures <i>Timo Henttonen, Microsoft</i>	Models for Improved Electroplating of TSV in 3DIC <i>Sridhar Narayanaswamy, Ph.D. Institute of High Performance Computing</i>	Challenges that the Semicon Industry gives X-Ray Technology and How we are working to Overcome them Keith Bryant, Yxlon International
11:00 AM	Chip Board Interaction Analysis of 22FDX® Wafer Level Packaging and Its Potential for System in Package Applications <i>Jae Cho, Ph.D., GlobalFoundries</i>	Wave Front Phase Imaging of Wafer Warpage <i>Jan Gaudestad, Wootix</i>	A Practical Guide for First-Time FOWLP Design Success <i>Keith Felton, Mentor, a Siemens Business</i>
11:30 AM	An Innovative Application of Fan-Out Packaging for Test & Measurement-Grade Products <i>Barrett Poe, Keysight Technologies</i>	High Density and High Bandwidth Chip-to-Chip Connections with 20µm pitch Flip-chip on Fan-Out Wafer-Level Package <i>Arnita Podpod, imec</i>	High Speed 3D Inspection of Advanced Package Interconnect Uniformity <i>Zonghu He, Rudolph Technologies</i>
12:00 PM	Wafer-Level Fan-Out for High-Performance, Low-Cost Packaging of Monolithic RF MEMS/CMOS <i>Rameen Hadizadeh, WiSpry</i>	Fabrication of a High Precision Magnetic Position Sensor based on a Through Silicon Via First Approach <i>Kai Zoschke, Fraunhofer IZM</i>	Design Trends and Challenges of Advanced Wafer-Level Manufacturing and Fanout <i>Bill Acito, IC Packaging Design Product Engineer Cadence Design Systems</i>
12:30 PM	LUNCH		
1:45 PM	<p style="text-align: center;"><b>KEYNOTE 2:</b>  <b>Monolithic versus Heterogeneous Packaging: Where Does the Future Lie?</b>  Walden Rhines, Ph.D., Mentor, a Siemens Business</p>		
	WLP Track	3D Track	Advanced Manufacturing Track
	Session 4: Advancements in WLP Integration Technology Chair: Tom Strothmann Co-Chair: Bora Baloglu	Session 5: Advanced Technologies Chair: Andy Heinig Co-Chair: Herb Reiter	Session 6: New Methods & Materials Chair: Garrett Oakes Co-Chair: Dale Gee
3:00 PM	Advanced eWLB (embedded Wafer Level Ball Grid Array) Solutions for mmWave Applications <i>SW Yoon, Ph.D., STATS ChipPAC</i>	Advanced RF Packaging Technology Trends, from WLP to 3D integration toward 5G and mmWave Application <i>Stéphane Elisabeth, Ph.D., System Plus Consulting</i>	Advancing Advanced Process Control in Backend Factories <i>Ben Williams, Applied Materials</i>
3:30 PM	Fan-out Wafer Processing in the High Density Packaging Era <i>David Butler, SPTS Technologies Ltd</i>	Antenna Integration Technologies for 5G Car-Application <i>Andy Heinig, Fraunhofer EAS</i>	Laser-Assisted Bonding and Debonding <i>Dirk Müller, Ph.D., Coherent</i>
4:00 PM	Heterogeneous Integration Challenges within Wafer Level Fan-Out SiP for Wearables and IoT <i>Eoin O'Toole, Amkor Technology Portugal, S.A</i>	Comparative Study of 3D Package Configurations in Power Delivery and Thermal Perspective <i>Heeseok Lee, Samsung Electronics</i>	Fine RDL Formation Using Alternative Patterning Solution for Advanced Packaging <i>Habib Hichri, Ph.D., sÜSS MicroTec Inc.</i>
4:30PM-6:00PM	NETWORKING RECEPTION		

### Wednesday, October 24

7:00 AM	REGISTRATION OPENS		
8:00 AM	CONTINENTAL BREAKFAST		
9:00 AM	<b>KEYNOTE: Interconnected World and the Automotive Paradigm</b> <i>Veer Dhandapani, Ph.D., NXP Semiconductors</i>		
10:00 AM	BREAK IN THE EXHIBIT HALL		
	WLP Track (Oak)	3D Track (Pine)	Test Track (Cedar)
	Session 7: Wafer Level Fan-Out Process & Metrology Chair: Tom Strothmann Co-Chair: Marion Volpert	Session 8: Processing & Materials Chair: John Duan Co-Chair: Akash Agrawal	Session 9: Process & Technology Chair: Dale Gee Co-Chair: Garrett Oakes
10:30 AM	Advanced Packaging Metrology and Lithography that Overcomes FOWLP/FOPLP Die Placement Error <i>Keith Best and Mike Marshall, Rudolph Technologies</i>	Improve Control amidst Die Shrink, 3D Package Complications Woo Young Han, P.E., Rudolph Technologies	Thermal Debonding and Warpage Adjust of FOWLP – a Crucial Step in the Evolution of Advanced Packaging? <i>Klemens Reitingner, ERS</i>
11:00 AM	Optical Run-Out Correction for Improved Lithography Overlay Accuracy for FOWLP Applications <i>Markus Arendt, SUSS MicroTec Photonic Systems Inc.</i>	Reducing the Cost of Applying Ultra-Thin, Package Level EMI Shield Coatings <i>Stuart Erickson, Ultrasonic Systems, Inc.</i>	Degas Module Thermal Architecture, Variable Wafer Delays, and Throughput, Productivity, and Consistency in Fan-Out Packaging <i>Barrier/Seed Layer PVD</i> <i>Paul Werbaneth, Intevac, Inc.</i>
11:30 AM	The Effective Solution for Wafer-Level Package Warpage Control by Low Temp Curable WLP Granule & Powder Encapsulation Materials <i>Junghwa Kim, Samsung SDI</i>	Plasma Coating and Protection of Wearable Devices <i>Simon McElrea, Semblant</i>	Significant Advancement in Laser Ablative Release Layer Material Design Enabling Low-Energy and Low-Residue Debond <i>Luke Prenger, Brewer Science</i>
12:00 PM	Exposed die Fan-Out Wafer Level Packaging by Transfer Molding <i>Wilfred Gal, Besi Netherlands B.V.</i>	Enabling Reliability of 3D TSV Advanced Packages with Non-Conductive, Pre-Applied Underfill Film Material <i>Jie Bai, Ph.D., Henkel Electronic Materials</i>	Failure Relief in FOWLP Polymer Layers <i>Robert Hubbard, Ph.D., Lambda Technologies, Inc.</i>
12:30 PM	LUNCH		
	WLP Track	3D Track	
	Session 10: Panel Level Fan-Out Packaging Chair: Marion Volpert Co-Chair: Jan Vardaman	Session 11: Wafer Bonding Applications Chair: Anup Pancholi Co-Chair : Akash Agrawal	
1:30 PM	Recent Developments in Panel Level Packaging <i>Tanja Braun, Dr.-Ing, Fraunhofer IZM</i>	Development of Low Temperature Direct Bond Interconnect Technology for Die- to-Wafer and Die-to-Die Applications—Stacking, Yield Improvement, Reliability Assessment <i>Guilian Gao, Ph.D., XPERI/Invensas</i>	
2:00 PM	Fabrication of Redistribution Structure Using Highly Reliable Photosensitive Polyimide for Fan Out Panel Level Packages <i>Hitoshi Araki, Ph.D., Toray Industries</i>	Temporary Bonding and the Challenge of Cleaning Post Debond <i>Kenji Nulman, Veeco Instruments</i>	
2:30 PM	Overcoming Critical Scaling Challenges in fine line RDL lithography and Plating Processes at Panel Scale <i>Robert Moon, TEL NEXX</i>	Collective Bonding for Heterogeneous Integration in Advanced Packaging Thomas Uhrmann, Ph.D., EV Group	
3:00 PM	Study of Fine Pitch RDL first FO-PLP/WLP <i>Hitoshi Onozeki, Hitachi Chemical</i>	The Road to Wafer-On-Wafer (WOW) High Volume Manufacturing (HVM) <i>Boris Kesil, Quartet Mechanics, Inc.</i>	
3:30 PM	BREAK IN EXHIBIT HALL		
4:00 PM	<b>PANEL DISCUSSION: What is the Sweet Spot for Large Area (Panel) Packaging</b> Moderators: Jan Vardaman, TechSearch International, Inc. & Tanja Braun, Dr.-Ing., Fraunhofer IZM Richard Bae, Samsung Electro-Mechanics Company (SEMCO) Thomas DeBonis, Intel John Hunt, ASE Markus Leitgeb, AT&S Tim Olson, Deca Technologies		
5:00 PM	Closing Comments		

### Thursday, October 25

Professional Development Courses		
	Donner Pass Ballroom	Siskiyou Ballroom
8:30 AM	PDC1: Fan Out Packaging - Technology Evolution John Hunt, ASE (US) Inc.	PDC2: Modeling Failure Modes for Chip package Interactions and Package Level Reliability Gil Sharon, DfR Solutions
1:30 PM	PDC3: Fan-Out Wafer/Panel-Level Packaging for 3D IC Heterogeneous Integration John Lau, Ph.D., ASM Pacific Technology	PDC4: Polymers and Processes Used in Wafer Level Packaging Jeffrey Gotro, Ph.D., InnoCentrix, LLC