IWLPC Sessions at a Glance

	Tuesday, October 24, 2017		
7:00am	**Registration Opens**		
	Session 1 WLP - 8:00am-10:00am (Oak) **WLP Materials** Chair: Luu Nguyen, Ph.D., Texas Instruments Co-Chair: Ron Legario, DuPont	**Session 2** 3D - 8:00am-10:00am (Pine) **Heterogeneous Integration Enablement** Chair: Herb Reiter, eda 2 asic Consulting Co-Chair: Laurette Nacamulli, Dow Chemical Co.	**Session 3** Advanced Manufacturing & Test - 8:00am-10:00am (Cedar) **Test** Chair: Ira Feldman, Feldman Engineering Corp. Co-Chair: Paul Werbaneth, Intevac, Inc.
8:00am	Low Temperature Curable PI/PBO for Wafer-Level Packaging *Daisaku Matsukawa, Ph.D., Hitachi Chemical DuPont MicroSystems, Ltd.*	Connectivity Management of Verticially Integrated Multi-Substrate Heterogeneous Packages *Kevin Rinebold, Mentor, a Siemens Business, John Ferguson, Mentor, Siemens Business and Magesh Govindarajan, Qualcomm Technologies*	Have you Designed for Manufacturing Test? *Gerard John, Amkor Technology*
8:30am	Enabling Fan-Out Wafer-Level Package (FOWLP) Through Innovative Lithography and Electrodeposition Technology *Justin Oberst, Lam Research*	Underfill Dispensing for Chip-On-Wafer *Akira Morita, Nordson Asymtek*	Contactor Materials & Impacts on Tip Wear & Life for WLCSP Testing *Frank Zhou, Smiths Interconnect*
9:00am	Wafer-Level Package Material and Process *Hitoshi Onozeki, Hitachi Chemical Co., Ltd.*	Application of Infrared Inspection to TCB and Die Placement Processes *Justin Brubaker, Kulicke & Soffa Industries*	Hybrid Copper Dielectric Direct Bonding of 200 mm CMOS Wafers with Five Metal Levels: Morphologic, Electrical and Reliability Characterization *Celso Cavaco, Ph.D., imec*
9:30am	Novel Low-temperature Curable Positive-Tone Photosensitive Dielectric Materials with High Elongation for Panel Level Package *Hitoshi Araki, Ph.D., Toray Industries, Inc.*	Comparison of Different Communication Interfaces between Chips Assembled onto Silicon Interposer *Andy Heinig, Fraunhofer IIS/EAS*	WLCSP Test Strategy *Michael Frazier, Xcerra Corporation*
10:00am	**Networking Break (10:00am-10:45am)** **Interactive Presentations (10:00am-1:30pm) |Bayshore Foyer** Chair: Garrett Oakes, EV Group Presenters: Interconnect Reuse Resolution and Verification with Bum Compensation for HDAP Designs Zain Ali, Mentor, a Siemens Business 3D Wafer Level Compression Molding Technology Development For CMOS Image Sensor Jim Zaccardi, FCI - Huatian Technologies Plasma Polymerization Applications for Advanced Wafer Level Packaging Abe Ghanbari, Ph.D., Semblant Low Temperature Multilayer EMI Shielding Brian Thomas, Evatec AG Application of Picosecond Ultrasonics for Advanced Packaging Process Monitoring and Control Tim Kryman, Rudolph Technologies Full Wafer Redistribution and Embedding as Key Technology for a Multi-Scale Neuromorphic Hardware Cluster Kai Zoschke, Fraunhofer IZM		
10:45am	**Welcome Comments** Oak Ballroom (2nd Floor) Curtis Zwenger, Amkor Technology, Inc. IWLPC General Chair		
11:00am	**KEYNOTE ADDRESS: The next step in Moore's law: Getting Rid of the Package and Replacing the Printed Circuit Board** (Oak Ballroom) *Subramanian Iyer, Ph.D.* *Distinguished Chancellor's Professor, University of California, Los Angeles* Chair: Curtis Zwenger, Amkor Technology, Inc. Co-Chair: Scott Hayes, NXP Manufacturing		
11:45am	**Lunch Break**		
	Session 4 WLP - 1:00pm-3:00pm (Oak) **WLP Processes** Chair: Steffen Kröhnert, Amkor Technology, Inc. Co-Chair: Jie Gong, Ph.D., KLA-Tencor	**Session 5** 3D - 1:00pm-3:00pm (Pine) **Novel Materials/Innovative Equipment** Chair: Sam Gu, Huawei R&D USA Co-Chair: Laurette Nacamulli, Dow Company Chemical Co.	**Session 6** Advanced Manufacturing & Test - 1:00pm-3:00pm (Cedar) **Productivity 1** Chair: Dale Gee, ON Semiconductor Co-Chair: Frank Zhou, Smiths Interconnect
1:00pm	The Thermocure System as A Technical Enabler for Wafer-Level Packaging Applications *Xiao Liu, Ph.D., Brewer Science Inc.*	Photo-Sensitive Insulation Film for Encapsulation and Embedding *Kiichi Fukuhara, Ph.D., Hitachi Chemical Co., Ltd.*	Rc Management for Next Generation PVD UBM/RDL Metallization Schemes *Anthony Barker, Ph.D., SPTS Technologies Ltd.*
1:30pm	Critical Process Parameters for DPSS Laser Debonding *Garrett Oakes, Ph.D., EV Group*	The Benefits of Source Die Input Flexibility in a TCB Process *Tom Strothmann, Kulicke & Soffa Industries*	Die-Level Traceability Using Adaptive Patterning *Craig Bishop, Deca Technologies*
2:00pm	Direct Write Lithography Approach for Wafer-Level Package *Hiroshi Matsui, SCREEN Semiconductor Solutions*	TMV Solutions Without Wet Chemistry *Catherine Shearer, Ormet Circuits, Inc.*	Temporary Bonding for High Temperature Processing of Willow Thin Glass *Robert Bellman, Ph.D., Corning, Inc.*
2:30pm	Electrical and Reliability of Ultra-fine Line Multi-Redistribution Layers Enabled by an Innovative Excimer Laser Dual Damascene Process for Wafer-Level Packaging *Habib Hichri, Ph.D., SUSS MicroTec Photonic Systems Inc.*	Toward a Flip-Chip Bonder Dedicated to Direct Bonding for Production Environment *Pascal Metzger, Ph.D., SET*	Transfer of Wafer-Level Packaging to Panel Format *Christian Onde, Ph.D., Atotech Deutschland GmbH*
3:00pm	**Networking Break** Exhibit Hall		
3:30pm	**Panel Discussion: Scaling Up Panel Level Processing: Challenges and Opportunities** Oak Ballroom (2nd Floor) Moderators: E. Jan Vardaman, TechSearch International, Inc. and Ira Feldman, Feldman Engineering Corp. Panelists: Tanja Braun, Ph.D., Fraunhofer IZM Michael Frazier, Xcerra Corporation Timothy Kryman, Rudolph Technology T.H. Kim, nepes Corporation Kazuo Yasuda, SCREEN, Kenny Igarashi, SCREEN		
4:15pm - 5:30pm	**Networking Reception**		

	Wednesday, October 25, 2017		
7:30am	**Registration Opens**		
8:30am	**KEYNOTE ADDRESS: Samsung's FOPLP: Beyond Moore** (Oak Ballroom) *Richard (Kwang Wook) Bae* *Vice President, Corporate Strategy & Planning, Samsung Electro-Mechanics* Chair: Chris Scanlan, Deca Technologies Co-Chair: Scott Hayes, NXP Manufacturing		
9:15am	**Networking Break** Exhibit Hall		
	Session 7 WLP -9:45am-11:45am (Oak) **Design and Process Technologies** Chair: Tom Strothmann, Kulicke & Soffa Industries Co-Chair: Luu Nguyen, Ph.D., Texas Instruments	**Session 8** 3D - 9:45am-11:45am (Pine) **Processing Technologies, Challenges and Schemes** Chair: Peter Ramm, Fraunhofer EMFT Co-Chair:Jeremy Theil, XPERI/Invensas	**Session 9** Advanced Manufacturing & Test- 9:45am-11:45am (Cedar) **Productivity 2** Chair: Garrett Oakes, EV Group Co-Chair: Dale Gee, ON Semiconductor
9:45am	New CAD Tools Feature for Virtual Prototyping *Tom Whipple, ZUKEN Inc.*	Fan Out eWLB Technology as an Advanced System-in-Package Solution *Vinayak Pandey, Ph.D.,STATS ChipPAC*	Wafer Thinning In-Line Inspection Process Control Solution for High Volume Manufacturing *Cleonisse Serrecchia, UnitySC*
10:15am	New Method for Embedding Power Semiconductors for Next Generation Electro-Mobility Requirements *James Welsh, Atotech Deutschland GmbH*	Integration of a Chemically-Amplified Photoresist and an Advanced Packaging Stepper for Advanced Packaging Technologies *Jack Mach, Rudolph Technologies*	Process and Productivity Results from a Carrier-Based Linear Transport PVD System for RDL Seed Layer Deposition in Fan-Out Packaging Applications *Paul Werbaneth, Intevac, Inc.*
10:45am	Fine Pitch Plating Resist for High Density FO-WLP *Hirokazu Sakakibara, JSR Corporation*	Development of Hybrid Bond Interconnect Technology for Die- to-Wafer and Die-to-Die Applications *Guilian Gao, Ph.D., XPERI/Invensas*	Fine Pitch Cu Pillar Assembly Challenges for Advanced Flip Chip Package *Vinayak Pandey, Ph.D., STATS ChipPAC*
11:15am	Heterogeneous Integration by Fan-Out Wafer-Level Packaging *John Lau, Ph.D., ASM Pacific Technology*	Dual side Chip Cooling Realized by Microfluidic Interposer Processing on 300mm Wafer Diameter *Wolfram Steller, Ph.D. Fraunhofer IZM ASSID*	TBA
11:45am	**Lunch Break**		
1:00pm	**KEYNOTE ADDRESS: Innovative Packaging Technologies Usher in a New Era for Integration Solutions** Oak Ballroom *Han Byung Joon, Ph.D.* *Group Chairman of Technology Strategy Committee, STATS ChipPAC* Chair: Chris Scanlan, Deca Technologies Co-Chair: Scott Hayes, NXP Manufacturing		
1:45pm	**Networking Break**		
	Session 10 WLP - 2:15pm-4:15pm (Oak) **Fan-Out WLP** Chair: Jan Vardaman, TechSearch International, Inc. Co-Chair: Steffen Kröhnert, Amkor Technology, Inc.	**Session 11** 3D - 2:15pm-4:15pm (Pine) **Smart System Integration and Applications** Chair: Jeremy Theil, Invensas Co-Chair: Sam Gu, Huawei R&D USA	**Session 12** Advanced Manufacturing & Test - 2:15pm-4:15pm (Cedar) **Inspection and Metrology** Chair: Gerard John, Amkor Technology, Inc. Co-Chair: Craig Bishop, Deca Technologies
2:15pm	Fan- Out WLP Technology as Sensor Packaging Solution *Jay Kim, Ph.D., nepes Corporation*	Technology Trends for Sensors using WLP and 3D TSV Integration *Romain Fraux, Systems Plus Consulting*	Advanced Packaging Inspection Solutions for FOPLP Processing *Benjamin Meihack, P.E., Rudolph Technologies*
2:45pm	Fan-Out Package Technology Based SiP for Advanced RF and High Performance Applications *Gaurav Sharma, GLOBALFOUNDRIES US Inc.*	Micro Thin-film Li-ion Battery Stacking Technology by Backside Via Last TSV for IoT Devices *Yasuhiro Morikawa, ULVAC, Inc.*	Optical Inspection Solutions for Fan Out Wafer and Panel-Level Packaging Modules *Shye Shapira, Ph.D., Camtek*
3:15pm	Challenges of Ball-Attach Process Using Flux for Fan Out Wafer/Panel Level Packaging *Yan Liu, Ph.D., Indium Corporation*	Integration for Mobile Security, A Secure Smart Card Application *René Puschmann, Fraunhofer IZM ASSID*	Challenges of ECD Fan Out in High Volume and Potential Solutions *Cristina Chu, TEL NEXX*
3:45pm	Fan Out Wafer and Panel Level Technology for Advanced LED Packaging *Tanja Braun, Ph.D. Fraunhofer IZM*	Package Assembly Design Kits - The Technology Bridge between Chip Design and Wafer-Level Manufacturing and Assembly *Jonathan Micksch, Amkor Technology, Inc.*	Inspection Challenges in Fan Out Level Packaging *Woo Young Han, P.E., Rudolph Technologies*
4:15pm	**Conference Ends**		

	Thursday, October 26, 2017		
	7:30am Registration Opens		
Workshop#	**Instructor**	**Time/Room**	**Topic**
WS1	John Hunt, ASE (US) Inc.	8:30am-12:00pm | San Martin	Fan Out Packaging - Technology Overview and Evolution
WS2	Fernando Roa, Ph.D. Amkor Technology	8:30am-12:00pm|San Carlos	Package on Package Design, Process and Quality
WS3	John Lau, Ph.D., ASM Pacific Technology	1:30pm-5:00pm | San Carlos	Fan-Out Wafer-Level Packaging and 3D Packaging
WS4	Rao Tummala, Ph.D., Georgia Institute of Technology	1:30pm-5:00pm | San Martin	Future of Packaging: Embedded and Non-Embedded Fan-Out