

IWLPC Sessions at a Glance

Tuesday, October 24, 2017			
7:00am	Registration Opens		
	Session 1 WLP - 8:00am-10:00am (Oak) WLP Materials Chair: Luu Nguyen, Ph.D., Texas Instruments Co-Chair: Ron Legario, DuPont	Session 2 3D - 8:00am-10:00am (Pine) Heterogeneous Integration Enablement Chair: Herb Reiter, eda 2asic Consulting Co-Chair: Laurette Nacamulli, Dow Chemical	Session 3 Advanced Manufacturing & Test - 8:00am-10:00am (Cedar) Test Chair: Ira Feldman, Feldman Engineering Corp. Co-Chair: Paul Werbaneth, Intevac
8:00am	Low Temperature Curable PI/PBO for Wafer-Level Packaging <i>Daisaku Matsukawa, Ph.D., Hitachi Chemical DuPont Microsystems, Ltd.</i>	Connectivity Management of Vertically Integrated Multi-Substrate Heterogeneous Packages <i>Keith Felton, Mentor Graphics and Magesh Govindarajan, Qualcomm Technologies</i>	Have you Designed for Manufacturing Test? <i>Gerard John, Amkor Technology</i>
8:30am	Enabling Fan-Out Wafer-Level Package (FOWLP) Through Innovative Lithography and Electrodeposition Technology <i>Bryan Buckalew, Lam Research</i>	Underfill Dispensing for Chip-On-Wafer <i>Akira Morita, Nordson Asymtek</i>	Contact Material & Impacts on Tip Wear & Life for WLCSP Testing <i>Jiachun(Frank) Zhou, Smiths Interconnect</i>
9:00am	Wafer-Level Package Material and Process <i>Hitoshi Onozeki, Hitachi Chemical Co., Ltd.</i>	Application of Infrared Inspection to TCB and Die Placement Processes <i>Justin Brubaker, Kulicke & Soffa Industries</i>	Hybrid Copper Dielectric Direct Bonding of 200 mm CMOS Wafers with Five Metal Levels: Morphologic, Electrical and Reliability Characterization <i>Celso Cavaco, Ph.D., imec</i>
9:30am	Novel Low-temperature Curable Positive-Tone Photosensitive Dielectric Materials with High Elongation for Panel Level Package <i>Hitoshi Araki, Ph.D., Toray Industries, Inc.</i>	Comparison of Different Communication Interfaces between Chips Assembled onto Silicon Interposer <i>Andy Heinig, Fraunhofer IIS/EAS</i>	WLCSP Test Strategy <i>Michael Frazier, Xcerra Corporation</i>
10:00am	Networking Break (10:00am-10:30am) Interactive Presentations (10:00am-1:30pm) Bayshore Foyer Chair: Garrett Oakes, EV Group Presenters: Interconnect Reuse Resolution and Verification with Bum Compensation for HDAP Designs Zain Ali, Mentor Graphics 3D Wafer Level Compression Molding Technology Development For CMOS Image Sensor Tony Curtis, FCI- Huatian Technologies Plasma Polymerization Applications for Advanced Wafer Level Packaging Abe Ghanbari, Ph.D., Semblant Low Temperature Multilayer EMI Shielding Andreas Erhart, Evatec AG Application of Picosecond Ultrasonics for Advanced Packaging Process Monitoring and Control Priya Mukundhan, Rudolph Technologies Full Wafer Redistribution and Embedding as Key Technology for a Multi-Scale Neuromorphic Hardware Cluster Kai Zoschke, Fraunhofer IZM		
10:45am	Welcome Comments Oak Ballroom (2nd Floor) Curtis Zwenger, Amkor Technology IWLPC General Chair		
11:00am	KEYNOTE ADDRESS: The next step in Moore's law: Getting Rid of the Package and Replacing the Printed Circuit Board (Oak Ballroom) <i>Subramanian Iyer, Ph.D.</i> Distinguished Chancellor's Professor, University of California, Los Angeles Chair: Curtis Zwenger, Amkor Technology		
11:45am	Lunch Break		
	Session 4 WLP - 1:00pm-3:00pm (Oak) WLP Processes Chair: Steffen Kröhnert, NANIUM, S.A. Co-Chair: Jie Gong, Ph.D., KLA-Tencor	Session 5 3D - 1:00pm-3:00pm (Pine) Novel Materials/Innovative Equipment Chair: Siquan (Sam) Gu, Huawei Co-Chair: Laurette Nacamulli, Dow Company	Session 6 Advanced Manufacturing & Test - 1:00pm-3:00pm (Cedar) Productivity 1 Chair: Dale Gee, ON Semiconductor Co-Chair: Frank Zhou, Smiths Interconnect
1:00pm	The Thermocure System as a Technical Enabler for Wafer-Level Packaging Applications <i>Xiao Liu, Ph.D., Brewer Science Inc.</i>	Photo-Sensitive Insulation Film for Encapsulation and Embedding <i>Kiichi Fukuhara, Ph.D., Hitachi Chemical Co., Ltd.</i>	Rc Management for Next Generation PVD UBM/RDL Metallization Schemes <i>Anthony Barker, Ph.D., SPTS Technologies Ltd.</i>
1:30pm	Critical Process Parameters for DPSS Laser Debonding <i>Thomas Uhrmann, Ph.D., EV Group</i>	The Benefits of Source Die Input Flexibility in a TCB Process <i>Tom Strothmann, Kulicke & Soffa Industries</i>	Die-Level Traceability Using Adaptive Patterning <i>Craig Bishop, Deca Technologies</i>
2:00pm	Direct Write Lithography Approach for Wafer-Level Package <i>Hiroshi Matsui, SCREEN Semiconductor Solutions</i>	TMV Solutions Without Wet Chemistry <i>Catherine Shearer, Ormet Circuits, Inc.</i>	Temporary Bonding for High Temperature Processing of Willow Thin Glass <i>Robert Bellman, Ph.D., Corning, Inc.</i>
2:30pm	Electrical and Reliability of Ultra-fine Line Multi-Redistribution Layers Enabled by an Innovative Excimer Laser Dual Damascene Process for Wafer-Level Packaging <i>Habib Hichri, Ph.D., SUSS MicroTec Photonic Systems Inc.</i>	Toward a Flip-Chip Bonder Dedicated to Direct Bonding for Production Environment <i>Pascal Metzger, Ph.D., SET</i>	Transfer of Wafer-Level Packaging to Panel Format <i>Christian Onde, Ph.D., Atotech Deutschland GmbH</i>
3:00pm	Networking Break Exhibit Hall		
3:30pm	Oak Ballroom (2nd Floor) Moderators: Jan Vardaman, TechSearch International, Inc. and Ira Feldman, Feldman Engineering Corp. Panelists: Timothy Kryman, Rudolph Technology T.H. Kim, nepes Corporation Kazuo Yasuda, SCREEN Tanya Braun, Fraunhofer IZM Michael Frazier, Xcerra Corporation		
4:15pm - 5:30pm	Networking Reception		

Wednesday, October 25, 2017			
7:30am	Registration Opens		
8:30am	KEYNOTE ADDRESS: Samsung's FOPLP: Beyond Moore (Oak Ballroom) <i>Richard (Kwang Wook) Bae</i> <i>Vice President, Corporate Strategy & Planning, Samsung Electro-Mechanics</i> Chair: Chris Scanlan, Deca Technologies		
9:15am	Networking Break Exhibit Hall		
	Session 7 WLP -9:45am-11:45am (Oak) Design and Process Technologies Chair: Tom Strothmann, Kulicke & Soffa Co-Chair: Luu Nguyen, Ph.D., Texas Instruments	Session 8 3D - 9:45am-11:45am (Pine) Processing Technologies, Challenges and Schemes Chair: Peter Ramm, Faunhofer EMFT Co-Chair: Jeremy Theil, Invensas	Session 9 Advanced Manufacturing & Test- 9:45am-11:45am (Cedar) Productivity 2 Chair: Garrett Oakes, EV Group Co-Chair: Shekar Krishnaswamy, Applied Materials
9:45am	New CAD Tools Feature for Virtual Prototyping <i>Tom Whipple, ZUKEN Inc.</i>	Fan Out eWLB Technology as an Advanced System-in-Package Solution <i>Jacinta Aman Lim, STATS ChipPAC</i>	Wafer Thinning In-Line Inspection Process Control Solution for High Volume Manufacturing <i>Cleonisse Serrecchia, UnitySC</i>
10:15am	Performance of Wafer-Level Interconnects in Metal-Embedded Chip Assembly (MECA) Technology <i>Florian Herrault, Ph.D., HRL Laboratories</i>	Integration of a Chemically-Amplified Photoresist and an Advanced Packaging Stepper for Advanced Packaging Technologies <i>Jack Mach, Rudolph Technologies</i>	Fine Pitch Cu Pillar Assembly Challenges for Advanced Flip Chip Package <i>Nokibul Islam, Ph.D., STATS ChipPAC</i>
10:45am	New Method for Embedding Power Semiconductors for Next Generation Electro-Mobility Requirements <i>Cassandra Melvin, Atotech Deutschland GmbH</i>	Development of Hybrid Bond Interconnect Technology for Die- to-Wafer and Die-to-Die Applications <i>Gullian Gao, Ph.D., Xperi</i>	Process and Productivity Results from a Carrier-Based Linear Transport PVD System for RDL Seed Layer Deposition in Fan-Out Packaging Applications <i>Paul Werbaneth, Intevac, Inc.</i>
11:15am	Fine Pitch Plating Resist for High Density FO-WLP <i>Hirokazu Sakakibara, JSR Corporation</i>	Dual side Chip Cooling Realized by Microfluidic Interposer Processing on 300mm Wafer Diameter <i>Wolfram Steller, Ph.D. Fraunhofer IZM ASSID</i>	Fast Automated Wafer-Level Test Scheme for In-Line Quick Functional Reliability <i>Krishna Mohan Chavali, GLOBALFOUNDRIES Inc.</i>
11:45am	Lunch Break		
1:00pm	KEYNOTE ADDRESS: Innovative Packaging Technologies Usher in a New Era for Integration Solutions Oak Ballroom <i>Han Byung Joon, Ph.D.</i> <i>Chief Executive Officer, STATS ChipPAC</i> Chair: Chris Scanlan, Deca Technologies		
1:45pm	Networking Break		
	Session 10 WLP - 2:15pm-4:15pm (Oak) Fan-Out WLP Chair: Jan Vardaman, TechSearch International, Inc. Co-Chair: Steffen Kröhnert, NANIUM, S.A.	Session 11 3D - 2:15pm-4:15pm (Pine) Smart System Integration and Applications Chair: Jeremy Theil, Invensas Co-Chair: Shiqun (Sam) Gu, Huawei	Session 12 Advanced Manufacturing & Test - 2:15pm-4:15pm (Cedar) Inspection and Metrology Chair: Gerard John, Amkor Technology Inc. Co-Chair: Craig Bishop, Deca Technologies
2:15pm	Fan- Out WLP Technology as Sensor Packaging Solution <i>Lewis (In-Soo) Kang, nepes Corporation</i>	Technology Trends for Sensors using WLP and 3D TSV Integration <i>Romain Fraux, Systems Plus Consulting</i>	Advanced Packaging Inspection Solutions for FOPLP Processing <i>Benjamin Meihack, P.E., Rudolph Technologies</i>
2:45pm	Fan-Out Package Technology Based SIP for Advanced RF and High Performance Applications <i>Gaurav Sharma, GLOBALFOUNDRIES US Inc.</i>	Micro Thin-film Li-ion Battery Stacking Technology by Backside Via Last TSV for IoT Devices <i>Yasuhiro Morikawa, ULVAC, Inc.</i>	Optical Inspection Solutions for Fan Out Wafer and Panel-Level Packaging Modules <i>Shye Shapira, Ph.D., Camtek</i>
3:15pm	Challenges of Ball-Attach Process Using Flux for Fan Out Wafer/Panel Level Packaging <i>Yan Liu, Ph.D., Indium Corporation</i>	Integration for Mobile Security, A Secure Smart Card Application <i>René Puschmann, Fraunhofer IZM ASSID</i>	Challenges of ECD Fan Out in High Volume and Potential Solutions <i>Cristina Chu, TEL NEXX</i>
3:45pm	Fan Out Wafer and Panel Level Technology for Advanced LED Packaging <i>Tanja Braun, Ph.D. Fraunhofer IZM</i>	Package Assembly Design Kits - The Technology Bridge between Chip Design and Wafer-Level Manufacturing and Assembly <i>Jonathan Micksch, Amkor Technology</i>	Inspection Challenges in Fan Out Level Packaging <i>Woo Young Han, P.E., Rudolph Technologies</i>
4:15pm	Conference Ends		

Thursday, October 26, 2017			
7:30am Registration Opens			
Workshop#	Instructor	Time/Room	Topic
WS1	John Hunt, ASE (US) Inc.	8:30am-12:00pm San Martin	Fan Out Packaging - Technology Overview and Evolution
WS2	Fernando Roa, Ph.D. Amkor Technology	8:30am-12:00pm San Carlos	Package on Package Design, Process and Quality
WS3	John Lau, Ph.D., ASM Pacific Technology	c	Fan-Out Wafer-Level Packaging and 3D Packaging
WS4	Rao Tummala, Ph.D., Georgia Institute of Technology	1:30pm-5:00pm San Martin	Future of Packaging: Embedded and Non-Embedded Format